NOT MEASUREMENT SENSITIVE

MIL-STD-1309D
12 February 1992
SUPERSEDING
MIL-STD-1309C
18 November 1983

MILITARY STANDARD

Definitions of Terms

for

Testing, Measurement and Diagnostics

AMSC N/A
AREA ATTS
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

FOREWORD

1. This military standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Naval Sea Systems Command, SEA 55Z3, Department of the Navy, Washington, DC 20362-5101 by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

3. Testing, measurement, and the use of diagnostic devices are a prerequisite for maintaining operational readiness of equipment used by the three services in the performance of their assigned tasks. In order to improve commun-ications and to facilitate coordination, key words or terms, more commonly used, are defined in this standard.

4. Not every testing, measurement and diagnostic term is listed. Oscilloscope, voltmeter and similar terms, which can be readily found in any standard technical dictionary, have been excluded. This document contains terms selected from the following sources:

SPECIFICATIONS

MIL-T-28800	- Test Equipment for Use with Electrical and Electronic Equipment, General Specifications for
AFGS-87256	- Generic Integrated Maintenance Diagnostics

STANDARDS

DOD-STD-100	- Engineering Drawing Practices (Chapter 700 - Definitions)
MIL-STD-415	- Test Provisions for Electronic Systems and Associated Equipment, Design Criteria for
MIL-STD-471	- Maintainability Demonstration (Demonstration and Evaluation of Equipment/System Built-in-Test/External Test/Fault Isolation/Testability Attributes and Requirements addendum)
MIL-STD-721	- Definitions of Terms for Reliability and Maintainability
MIL-STD-1364	- Standard General Purpose Electronic Test Equipment
MIL-STD-1388	- Logistics Support Analysis (Appendix B, Glossary)
MIL-STD-2077	- General Requirements Test Program Sets
DOD-STD-2121	- Determination of Electronic Test Equipment Parameters
MIL-STD-2165	- Testability Program for Electronic Systems and Equipments

OTHER

AR 750-43 - Test, Measurement, and Diagnostic Equipment

Joint DARCOM/NMC/AFLC/AFSC/Commanders Selection Guide for Digital Test Program Generation Systems

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)/INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC. (IEEE)

100-1974 - Dictionary of Electrical and Electronics Terms
100-1988 - Dictionary of Electrical and Electronics Terms
416-1984 - ATLAS Test Language
716-1985 - C/ATLAS Test Language

CONTENTS

1. SCOPE

1.1 Purpose. The purpose of this standard is to standardize the definitions of the most commonly used terms for testing, measurement and diagnostics.

1.2 Scope. This standard establishes the definitions most commonly used for test, measurement and diagnostics.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-T-28800 - Test Equipment for Use with Electrical and Electronic Equipment, General Specifications for

STANDARDS

MILITARY

MIL-STD-1839 - Calibration and Measurement Requirements
MIL-STD-2077(NAVY) - General Requirements Test Program Sets
MIL-STD-7935.1-S - Automated Data Systems Documentation Standards
MIL-STD-38793 - Technical Manuals: Preparation of Calibration Procedures
MIL-STD-45662 - Calibration Systems Requirements

2.2 Non-Government publications. The following documents form a part of this standard to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted shall be those listed in the issue of DoDISS specified in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issued of the documents cited in the solicitation (see 6.2).

IEEE Std 416-1984 - IEEE Standard ATLAS Test Language
716-1989 - C/ATLAS Test Language

(Application for copies should be addressed to the Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document shall take precedence. Nothing in this document, however, supersedes appli-cable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Definitions of terms used in this standard. The following defini-tions shall apply to the terms stated.

3.1.1 Absolute error. The magnitude of the error without regard to algebraic sign.

3.1.2 Absolute measurement. The measurement in which the comparison is directly with quantities whose units are basic units of the system. Notes: (a) For example, the measurement of speed by measurements of distance and time is an absolute measurement, but the measurement of speed by a speedometer is not an absolute measurement. (b) The word absolute implies nothing about precision or accuracy.

3.1.3 Accelerated life test. A test in which certain factors, such as voltage, temperature, and so forth, are increased or decreased beyond normal operating values to obtain observable deterioration in reasonable period of time, and thereby afford some measure of the probable life under normal operating conditions or some measure of the durability of the equipment when exposed to the factors being aggravated.

3.1.4 Acceptance test. A test to verify if the unit under test (UUT) is operating in accordance with the operational specifications.

3.1.5 Accessory. (1) An accessory is an assembly of a group of parts or a unit which is not always required for the operation of a test set or unit as originally designed but serves to extend the functions or capabilities of the test set; similarly as headphones for a radio set supplied with a loud-speaker, a vibrator power unit for use with a set having a built-in power supply, or a remote control unit for use with a set having integral controls. (2) A part, subassembly, or assembly designed for use in conjunction with or to supplement another assembly, or a unit or set, contributing to the effectiveness thereof without extending or varying the basic function of the assembly or set. An accessory may be used for testing, adjusting, or cali-brating purposes. (Examples: test instrument, recording camera for radar set, headphones, emergency power supply).

3.1.6 Accuracy. (1) The quality of freedom from mistake or error, that is, of conformity to truth or to a rule. Notes: (a) Accuracy is distinguished from precision as in the following example: A six-place table is more precise than a four-place table. However, if there are errors in the six-place table, it may be more or less accurate than the four-place table. (b) The accuracy of an indicated or recorded value is expressed by the ratio of the error of the indicated value to the true value. It is usually expressed in percent. Since the true value cannot be determined exactly, the measured or calculated value of highest available accuracy is taken to be the true value or reference value. Hence, when a meter is calibrated in a given echelon, the measurement made on a meter of a higher-accuracy

echelon usually will be used as the reference value. Comparison of results obtained by different measurement procedures is often useful in establishing the true value. (2) The degree of correctness with which a measured value agrees with the true value.

3.1.7 Accuracy augmentation routine. Test routines using auxiliary test equipment that is more accurate than the automatic test equipment complement, as may be necessary when test accuracy ratios cannot be met otherwise.

3.1.8 Accuracy enhancement. A process which provides accuracies beyond the individual instrument capability by monitoring the instrument performance with another instrument of much greater accuracy over the duration of the test, or by means of software algorithms.

3.1.9 Accuracy rating. The accuracy classification of the instrument. It is given as the limit, usually expressed as a percentage of full-scale value of reading or of programmed value, that errors will not exceed when the instrument is used under reference conditions.

3.1.10 Acquisition time. The time required for a test and measurement system to acquire an input signal, the minimum time needed to accurately measure the applied input.

3.1.11 Active built-in-test (BIT). A type of BIT which periodically disrupts the prime system operation through the injection of test stimuli into the system. Also referred to as BIT, active.

3.1.12 Active redundancy. That condition where parallel back-up items are operating simultaneously, rather than being switched on when needed.

3.1.13 Active sensor. (1) A sensor requiring a source of power other than the signal being measured. (2) A sensor that provides a signal by stimulating the UUT.

3.1.14 Active testing. The process of determining equipment static and dynamic characteristics by performing a series of measurements during a series of known operating conditions. Active testing may require an interruption of normal equipment operations and it involves measurements made over the range of equipment operation.

3.1.15 Adapter. (1) A device for connecting parts that will not mate. An accessory to convert a device to a new or modified use. (2) A device or series of devices designed to provide a compatible connection between the unit under test and the test equipment. May include proper stimuli or loads not contained in the test equipment.

3.1.16 Adapter kit. A kit containing an assortment of cables and adapters for use with test or support equipment.

3.1.17 Adjust. Change the value of some element of the mechanism, or the circuit of the instrument or of an auxiliary device, to bring the indication to a

desired value, within a specified tolerance for a particular value of the quantity measured.

3.1.18 Adjustment. Changing (by electronic, electrical or physical means) a variable in an item to cause a change in its output characteristics.

3.1.19 Algorithmically generated pattern. An array of digital data automatically generated by a predetermined software routine or program. The pattern may be generated and applied in real time.

3.1.20 Align. To adjust a circuit, equipment or system so that their functions are properly synchronized or their relative positions properly oriented. For example, trimmers, padders, or variable inductances in tuned circuits are adjusted to give a desired response for fixed tuned equipment or to provide tracking for tuneable equipment.

3.1.21 Alignment. Performing the adjustments that are necessary to return an item to specified operation.

3.1.22 Alignment kit. A set of instruments or tools necessary for the adjustment of electrical or mechanical components.

3.1.23 Alignment program. A program used to align instruments and signal paths to known characteristics.

3.1.24 Ambiguity delay. A delay model which allows the minimum and maximum propagational delay through an element to be specified. The state of the element between minimum and maximum delay is unknown, and is called the ambiguity region.

3.1.25 Ambiguity group. (1) A group of replaceable items which may have faults resulting in the same fault signature. (2) The group of items to which a given fault is isolated, any one of which may be the actual faulty item.

3.1.26 Analog. Data in the form of continuously variable quantities, such as voltage, frequency, current, etc.

3.1.27 Analog computer. A computer which represents variables by existing analogies. Thus, a computer which solves problems by translating existing conditions such as flow, temperature, pressure, angular position or voltage into related mechanical or electrical equivalent quantities as an analog for the existing phenomenon being investigated. In general, it is a computer which uses an analog for each variable and produces analog as outputs. Thus, an analog computer measures continuous quantities whereas a digital computer operates on discrete data.

3.1.28 Ancillary equipment. Equipment which is auxiliary or supplementary to prime equipment installation. Ancillary equipment usually consists of standard off-the-shelf items such as an oscilloscope or distortion analyzer.

3.1.29 Aperture delay. The time elapsed from the hold command to when the switch actually opens.

3.1.30 Aperture uncertainty. The time variation from sample to sample of the aperture delay.

3.1.31 Approved equipment test procedure. The test procedure furnished by the Government or furnished by a contractor in accordance with the requirements of the contract or order and approved by the Government in accordance with the contract or order.

3.1.32 Architecture. A method or style of building a system (hardware or software). The construction, frame or structure of that system.

3.1.33 ATE bit skew. The maximum time difference between the first and last digital pulse arriving at the ATE interface within the same digital test pattern.

3.1.34 ATE control software. Software used during execution of a test program which controls the nontesting operations of the ATE. This software is used to execute a test procedure but does not contain any of the stimuli or measurement parameters used in testing the UUT. Where test software and control software are combined in one inseparable program, that program will be treated as test software not control software.

3.1.35 ATE oriented language. A computer language used to program an automatic test equipment to test UUTs, whose characteristics imply the use of a specific ATE system or family of ATE systems.

3.1.36 ATE support software. Computer programs which aid in preparing, analyzing, and maintaining test software. Examples are: ATE compilers, translation analysis programs, and punch/print programs.

3.1.37 ATE system software. The total software environment of the ATE including operating system, test executives, user interface, system self-test, and other software required to run test programs. This does not include test programs for supported end items.

3.1.38 ATLAS. A standard abbreviated English language used in the preparation and documentation of test procedures which can be implemented either manually or with automatic or semi-automatic test equipment. ATLAS is controlled by the Institute of Electrical and Electronics Engineers (IEEE) Standards Coordinating Committee 20 (SCC 20).

3.1.39 ATLAS-Ada Based Environment for Test (ABET). An Ada environment which interfaces to and supports the application of the IEEE P1226 family of standards centered in the test domain.

3.1.40 ATLAS vocabulary. The range of words and symbols used in standard ATLAS.

3.1.41 Automatic built-in test (ABIT). A subset of BIT which is initiated automatically when subsystem electrical power is turned on; it provides continuous or iterative testing and monitoring, is non-interruptive to normal system operation (following the initial power-up tests) and invisible to the operator except when a

operator-relevant fault is detected and reported; detects and isolates each fault to the corresponding level of maintenance.

3.1.42 Automatic check-out equipment (ACE). An equipment designed to check functional parameters and to perform fault isolation of item malfunctions.

3.1.43 Automatic monitoring equipment (AME). An equipment that is designed to automatically conduct analysis of function or degradation.

3.1.44 Automatic self-test. Self-test to that degree of fault detection and isolation which can be achieved entirely under computer control, without human intervention. May be operator initiated or ABIT.

3.1.45 Automatic self-calibration. The capability of a test system to automatically check its own accuracy by means of internal standards, the internal standards being calibrated using external means.

3.1.46 Automatic test. That performance assessment, fault detection, diagnosis, isolation, and prognosis which is performed with a minimum of reliance on human intervention. This may include BIT.

3.1.47 Automatic test equipment (ATE). (1) Test, measurement and diagnostic equipment (TMDE) that performs a program to test functional or static parameters, to evaluate the degree of performance degra-dation, or to perform fault isolation of unit malfunctions. The decision making, control, or evaluative functions are conducted with minimum reliance on human intervention. (2) An equipment that is designed to automatically conduct analysis of functional or static parameters, evaluate the degree of performance degradation and perform isolation of item malfunctions.

3.1.48 Automatic test program generator (ATPG). A generic computer program which automatically generates the test patterns and responses from UUT circuit configuration information. Also known as auto-matic test generator.

3.1.49 Automatic test system. ATE, associated system software, all items required for support, and those supported end item test program sets that may be used with the ATE.

3.1.50 Automatic testing. That discipline which concerns itself with the development, acquisition, and application of automatic test.

3.1.51 Auxiliary equipment. Equipment which is supplementary to a prime equipment installation. Auxiliary equipment usually consists of standard off-the-shelf items such as oscilloscopes and distortion analyzer. Also called ancillary equipment.

3.1.52 Availability. A measure of the degree to which an item is in an operable and committable state at the start of a mission, when the mission is called for at an unknown (random) point in time.

3.1.53 Back driving. The process of forcing a logic level onto the output of a device that differs from the level it is attempting to drive.

3.1.54 Back trace. The process of tracing back from the failure site to the primary inputs and making an input assignment so that a distinguishable test can be produced at the failure site.

3.1.55 Backdrive. Informal term describing the high current/short duration stimulus used to isolate digital devices for in-circuit test.

3.1.56 Backus-Naur form (BNF). A particular metalanguage developed by Backus and Naur.

3.1.57 Basic element. A measurement component or group of components that performs one necessary and distinct function in a sequence of measurement operations. Note: Basic elements are single-purpose units and provide the smallest steps into which the measurement sequence can be classified conveniently. Typical examples of basic elements are: a permanent magnet, a control spring, a coil, and a pointer and scale.

3.1.58 Basic reference standards. Those standards used to maintain physical and electrical units in the laboratory, and which serve as the starting point of the chain of sequential measurements carried out in the laboratory.

3.1.59 Bed of nails interface adapter. A type of interface adapter which uses a series of pogo-pins or nails to make contact with the UUT.

3.1.60 Benchmark. A test point for comparison purposes; in microprocessor-based equipment, a benchmark program is one used to compare aspects of performance among competing systems.

3.1.61 Bidirectional bus. A conductor or group of conductors which transmits and receives digital data on the same line(s).

3.1.62 Binary simulator. A program which establishes a representation of a logic circuit or configuration based upon a computer-directed or processed model of the logic circuit or configuration.

3.1.63 BIT turn-on. A specific type of initiated BIT which is exercised each time power is applied to the unit or system. Also referred to as turn-on BIT.

3.1.64 Block input. (1) A section of internal storage of a computer, reserved for the receiving and processing of input information (synonymous with "input area"). (2) A block used as an input buffer. (3) A block of machine words considered as a unit and intended to be transferred from an internal storage medium to a computer.

3.1.65 Block output. (1) A section of internal storage, reserved for storing data which are to be transferred out of the computer. (2) A block used as an output buffer. (3) A block of machine words considered as a unit and intended to be transferred from an internal storage medium to a computer.

3.1.66 Branch logic isolation time. Branch logic isolation time is the time required to follow the worst case logic chain of each diagnostic branch containing three or more unique tests.

3.1.67 Breakdown. A disruptive discharge through insulation, involving a sudden and large increase in current due to failure of the insulation under electrical voltage stress.

3.1.68 Bridge fault. Short circuits or leakage between adjacent paths (lands, traces) on a printed circuit board (card).

3.1.69 Buffer. An isolating circuit used to avoid reaction of a driven circuit on the corresponding driving circuit.

3.1.70 Building block. A measurement or stimulus device, usually programmable, such as a multimeter, power supply, switching unit, or frequency meter, installed as an integral part of the test equipment.

3.1.71 Built-in-test (BIT). A test approach using built-in test equipment or self-test hardware and software that is internally designed into the supported end item to test all or a part of that item.

3.1.72 Built-in-test equipment (BITE). Any identifiable device that is a part of the supported end item and is used for testing that supported end item.

3.1.73 Burn-in. The operation of items prior to their end application to stabilize their characteristics and precipitate early failures.

3.1.74 Burst. A pulse train that starts at a prescribed time and continues for a specified duration (or number of pulses).

3.1.75 Bus. A conductor, or group of conductors, which serve as the path for carrying digital control, address, and information signals. Also power distribution between controlling and controlled electronic items.

3.1.76 Bus-structured architecture. Circuit design incorporating a microprocessor and related devices operating in conjunction, and interconnected by several parallel electrical lines: the bus.

3.1.77 C/ATLAS. A high order language defined by IEEE Standard 716 Abbreviated Test Language for All Systems (ATLAS) which is used for the writing of test programs for UUTs, so that these programs can operate on various makes and models of ATE.

3.1.78 Calibration. The comparison of a measurement system or device of unverified accuracy with a measurement system of known and greater accuracy to detect and correct any deviation from required performance specifications of the unverified measurement system or device.

3.1.79 Calibration adapter. An interface adapter which may include precision active circuits to aid in ATE self certification, or to verify calibration of ATE instruments or functions, and building blocks.

3.1.80 Calibration interval. The maximum length of time between calibration services during which a specified percentage of equipment is expected to remain within acceptable performance levels under normal conditions of handling and use.

3.1.81 Calibration procedure. The specific steps and operations to be followed by activity personnel in the performance of an instrument calibration.

3.1.82 Calibration procedure instruction (CPI). A written document providing the information needed for calibrating an ATE or individual instrument, list of calibration standards, test methods description, test tolerances and other calibration procedure preparation information.

3.1.83 Calibration test program (CTP). A computer program designed to calibrate an ATE or individual instrument.

3.1.84 Calibration test program set (CTPS). A complete set of CTP, CPI, information and supplementary data developed for the purpose of calibrating an ATE or individual instrument.

3.1.85 Cam-programmed. (1) A programming technique that uses a rotating shaft, having specifically oriented, eccentric projections which control a series of switches that set up the proper circuits for a test. (2) A cam-follower system used to set positions or values of a shafted instrument for programming instructions to the test system.

3.1.86 Cannot duplicate (CND). An operationally observed/recorded system malfunction (for example, by BIT or on-line monitoring means) which maintenance personnel were unable to duplicate.

3.1.87 Card tester. An instrument for testing and diagnosing printed circuit cards.

3.1.88 Catastrophic failure. A failure mode which is both sudden and complete. This failure causes cessation of one or more fundamental functions.

3.1.89 Catastrophic fault. A physical condition causing a catastrophic failure.

3.1.90 Central integrated test system. An on-line test system which processes, records, or displays at a central location, information gathered by test point data sensors at more than one remotely located equipment or system under test (also called system integrated test system).

3.1.91 Centralized test system. A test system, which processes, records or displays at a central location, information gathered by test point data sensors at more than one remotely located equipment or system under test.

3.1.92 Certification. Verification that a support test system is capable, at the time of certification demonstration, of correctly assessing the quality of the items to be tested. This verification is based on an evaluation of all support test system elements and establishment of acceptable correlation among similar test systems.

3.1.93 Certification time. Certification time includes all time required to check the equipment parameters on all range and function settings and all inputs

and outputs. Certification time does not include the time to repair and readjust the equipment as a result of a malfunction.

3.1.94 Channel. A single path for transmitting electrical signals, usually in distinction from other parallel paths.

3.1.95 Check routine. A routine or program designed to provide information about the operational condition of a computer or computer control system. Generally, a check routine is designed to give the operator of the system a high confidence level that the equipment is operating properly (also called check program).

3.1.96 Checkout. Tests or observations of an item to determine its condition or status.

3.1.97 Checkout equipment. Electric, electronic, optical, mechanical, hydraulic, or pneumatic equipment, either automatic, semiautomatic, or manual, or any combination thereof, which is required to perform the checkout function.

3.1.98 Checkout time. The time required to determine whether designated characteristics of a system are within specified values.

3.1.99 Checkpoint. A place in a routine where a check, or a recording of data for restart purposes, is performed.

3.1.100 Checksum. The sum of every byte contained in an input/output (I/O) record or memory used for assuring integrity of the programmed entry.

3.1.101 Circuit. A conductor, or system of conductors, and active or passive elements through which an electric current is intended to flow to produce a specific electrical or electronic function.

3.1.102 Circuit card tester. An instrument for testing and diagnosing printed circuit cards.

3.1.103 Circuit image. The representation of the functions and interconnections of an electronic circuit in a format compatible with the ATPG system being used.

3.1.104 Circuit load. (1) The amount of power drawn from a circuit. (2) A device or an electronic circuit which provides a simulation of the normal I/O loads of the circuit under test.

3.1.105 Circuit malfunction analysis. The logical, systematic examination of circuits and their diagrams to: (a) identify and analyze the probability and consequence of potential malfunctions; and (b) to determine related maintenance and support requirements to investigate effects of failures (allied with failure modes and effects analysis (FMEA)).

3.1.106 Circuit simulator. A computer program which simulates the operation of an electronic circuit. In digital applications, it also analyzes the efficiency of stimulus test patterns on itself.

3.1.107 Clock. A device that generates periodic signals used for synchronization.

3.1.108 Closed loop testing. Testing in which the input stimulus is controlled by the equipment output monitor.

3.1.109 Coding. That part of the test program development process where the test sequences are translated into the language of the ATE controller.

3.1.110 Command. An electronic pulse, signal, or set of signals to start, stop, change, or continue some operation.

3.1.111 Common mode noise. The noise voltage which appears equally and in phase from each signal conductor to ground.

3.1.112 Common mode noise rejection. The ability to reduce common mode potential in a floating measurement system.

3.1.113 Common mode rejection ratio. The ratio of differential voltage gain to common mode voltage gain, usually expressed in decibels.

3.1.114 Common support equipment. That support equipment which is applicable to several systems, subsystems, or items of equipment.

3.1.115 Comparative test. Comparative tests compare end item signal or characteristic values against a specified tolerance band and present the operator with a go or no-go readout; a "go" for signals within tolerances, and a "no-go" for signals out-of-tolerance.

3.1.116 Comparator. (1) A device capable of comparing a measured value with predetermined limits to determine if the value is within these limits. (2) A device capable of comparing digital signals to determine agreement.

3.1.117 Comparison tester. A device which uses a known good unit (golden unit) as a means for comparing test results with the UUT when both are subjected to the same stimuli.

3.1.118 Compatibility. (1) Design features of a UUT which provide functional, electrical, and mechanical interfacing with the intended ATE and which minimize the use of unique or complex interface devices. (2) The condition which exists when test results are usable and consistent across different levels of maintenance (also referred to as vertical test compatibility).

3.1.119 Compiler. A computer program which translates high order language instructions of a computer program into machine language before the instructions are executed (for example, BASIC to machine code).

3.1.120 Compiler-driven simulation. The simulation carried out by translation of the network description into machine executable code. This technique is employed for clocked (synchronous) networks and primitive blocks.

3.1.121 Complete operating test equipment. Equipment together with the necessary detail parts, accessories, and components, or any combination thereof, required for the testing of a specified operational function.

3.1.122 Comprehensive testability. An overall testability design characteristic which includes both hardware design and test design.

3.1.123 Computer assisted tester. A tester not directly programmed by a computer but which operates in association with a computer by using some arithmetic functions of the computer.

3.1.124 Computer-guided probe. A fault isolation technique based solely on the good circuit data. The probe algorithm acts as the master instruction operator to probe various integrated circuit pins on the UUT until it derives the final diagnosis and diagnostics.

3.1.125 Concurrent fault simulation. Fault simulation is deduced by the propagation of super fault lists during a single pass simulation. A super fault list of a primitive building block is composed of the faults that affect at least one of its input or output values, and of the input/output values for the faults. Concurrent simulation is applicable to functional level processing.

3.1.126 Cone of tolerance. The specification of tighter test tolerances at the factory (or at component or subassembly indenture levels) which gradually loosen at successive main-tenance levels (or higher assembly indenture levels, system level being the highest.) Also known as inverted pyramid. The use of a cone of tolerance approach tends to reduce RTOK problems.

3.1.127 Confidence test. (1) A test performed to provide a high degree of certainty that the UUT is operating acceptably. (2) A check of the performance of all test system stimulus and measurement functions, to detect degradation with respect to system specifications, and to inform the system operator.

3.1.128 Conformance tests. Tests that are specifically made to demonstrate conformity with applicable standards or specifications.

3.1.129 Contact. (1) A connection between two conductors that permits a current flow path. (2) A part or device that makes or breaks a current patch connection.

3.1.130 Continuity test. A test for the purpose of detecting broken or open connections and ground circuits in a network or device.

3.1.131 Continuity tester. An electrical tester used to determine the presence and location of broken or open connections and grounded circuits.

3.1.132 Continuous BIT. A type of BIT which continually monitors system operation for errors. Also referred to as BIT, continuous.

3.1.133 Control panel. That part of ATE which includes the means by which the operator can control the ATE functions.

3.1.134 Control point. A design attribute to enhance testability by enabling, disabling, blocking, resetting and so forth, functions within a system to insert test stimulus and effect efficient test control.

3.1.135 Control point selector. A device capable of selecting and controlling the proper stimulus, power or load, and applying it to the UUT, in accordance with instructions from the programming device.

3.1.136 Controllability. An attribute of equipment design which defines or describes the extent to which signals of interest may be controlled.

3.1.137 Controller. A hardware interface that accepts instructions from a computer and reformats them to program an instrument or peripheral.

3.1.138 Converter. (1) A device which changes the manner of representing information from one form to another. (2) A machine or device for changing electrical energy from one form to another.

3.1.139 Corrective maintenance. (1) The maintenance carried out after a failure has occurred and intended to restore an item to a state in which it can perform its required function. (2) Actions performed to restore a failed or degraded equipment. It includes fault isolation, repair or replacement of defective circuit cards or components alignment and checkout.

3.1.140 Correlation. A portion of certification which establishes the mutual relationships between similar support test systems by comparing test data on specimen hardware or simulators.

3.1.141 Crest factor. The ratio of a signal's peak voltage level either positive or negative (whichever is greater) to its root-mean-square value.

3.1.142 Critical failure. A failure, or combination of failures, that prevents an item from performing a specified mission or puts human life at risk.

3.1.143 Critical race condition. The nearly concurrent change of two or more lines which may result in any one of two or more stable states being entered.

3.1.144 Criticality. A relative measure of the consequence of a failure mode and its frequency of occurrences.

3.1.145 Cross coupling. The amount of undesired energy appearing in one signal path as a result of coupling from other signal paths. Also referred to as crosstalk.

3.1.146 Crossbar switch/crossbar scanner. An electrical or electronic device having a plurality of "n" vertical paths and "m" horizontal paths, establishing "n" times "m" crosspoints or interconnections for the cross-switching of data circuits consisting of signal data, power, modifiers, or monitors for the purpose of injecting, altering, monitoring, or comparing information for test analyses. The switching may be accomplished by relays, tubes, transistors or diodes under manual or automated control. The scanner scans each sensor point during the measure and compares actions of the test equipment.

3.1.147 Crosstalk. The amount of undesired energy appearing in one signal path as a result of coupling from other signal paths. Also referred to as cross coupling.

3.1.148 Damping. Term applied to the performance of an instrument to denote the manner in which the pointer settles to its steady indication after a change in the value of the measured quantity. Two general classes of damped motion are distinguished as follows: (a) periodic (underdamped) in which the pointer oscillates around the final position before coming to rest, and (b) aperiodic (overdamped) in which the pointer comes to rest without overshooting the rest position. The point of change between periodic and aperiodic damping is called critical damping. Note: An instrument is considered for practical purposes to be critically damped when overshoot is present but does not exceed an amount equal to one-half the rated accuracy of the instrument.

3.1.149 Debug. (1) To examine or test a procedure, routine, or equipment for the purpose of detecting and correcting errors. (2) To detect, locate, and remove mistakes from a routine or malfunctions from a computer.

3.1.150 Debugging. A process to detect and remedy inadequacies. Not to be confused with terms such as burn-in, fault isolation or screening.

3.1.151 Dedicated switching. The property of a switching matrix which allows each device in a test system to connect to a unique point on the output.

3.1.152 Deductive fault simulation. Fault simulation is deduced by care-ful network analysis during a single pass simulation. For each node there is a list of faults that cause a different circuit response than the good circuit. The fault lists are propagated either through the Boolean operations of the primitive building blocks (fault list analysis) or by simulation of the logic differences (concurrent simulation).

3.1.153 Delay fault. A fault in digital device such that switching occurs to the proper level but does so outside of a specified time interval. Also referred to as a fault, delay.

3.1.154 Delay line. A transmission line or equivalent device designed to delay a signal for a predetermined length of time.

3.1.155 Delay line storage. A storage or memory device consisting of a delay line and means for regenerating and reinserting information into the delay line.

3.1.156 Dependability. A measure of the degree to which an item is operable and capable of performing its required function at any (random) time during a specified mission profile, given time availability at the start of the mission. (Item state during a mission includes the combined effects of the mission related system Reliability and Maintainability (R&M) parameters but excludes non-mission time).

3.1.157 Dependency Matrix. A Boolean Matrix which reflects the inter-dependency of components and tests in a given system configuration.

3.1.158 Dependent failure. A failure which is caused by the failure of an associated item, distinguished from independent failure. Also referred to as failure, dependent.

3.1.159 Dependent fault. A fault which is caused by the failure of an associated element.

3.1.160 Dependent node. A node having one or more incoming branches.

3.1.161 Depot maintenance. Maintenance performed on material requiring major overhaul or a complete rebuild of parts, subassemblies, and end items, including the manufacture of parts, modification, testing, and reclamation as required. Depot maintenance, serves to support lower categories of maintenance by providing technical assistance and performing that maintenance beyond their responsibility. Depot maintenance provides stocks or serviceable equipment by using more extensive facilities for repair than are available in lower level maintenance activities.

3.1.162 Design fault. A fault due to inadequate hardware or software design. Also referred to as a fault, design.

3.1.163 Design for testability. A design process or characteristic thereof such that deliberate effort is expended to assure that a product may be thoroughly tested with minimum effort, and that high confidence may be ascribed to test results.

3.1.164 Destructive testing. (1) Prolonged endurance testing of equipment or a specimen until it fails in order to determine service life or design weakness. (2) Testing in which the preparation of the test specimen or the test itself may adversely affect the life expectancy of the UUT or render the sample unfit for its intended use.

3.1.165 Detectable failures. Failures that can be identified through a periodic testing or can be revealed by alarm or anomalous indication. Component failures which are detected at the channel, division, or system level are detectable failures. Note: Identifiable but nondetectable failures are failures identifiable by analysis that cannot be detected through periodic testing or cannot be revealed by alarm or anomalous indication.

3.1.166 Diagnosis. The functions performed and the techniques used in determining and isolating faults.

3.1.167 Diagnostic accuracy. The percentage of failures correctly diagnosed, based on the possible failure population.

3.1.168 Diagnostic capability. All capabilities associated with the detection, isolation, and reporting of faults, including testing, technical information, personnel, and training.

3.1.169 Diagnostic effectiveness. A measure of the degree to which the diagnostic element(s) meets required fault detection and isolation levels.

3.1.170 Diagnostic efficiency. A measure of the ability of the diagnostic element(s) to effect required fault detection and isolation with a minimum of effort and expense. Diagnostic efficiency may be expressed as a ratio of diagnostic effectiveness to cost.

3.1.171 Diagnostic element. Any distinct, single part of the diagnostic capability.

3.1.172 Diagnostic flow chart. A test oriented logical description of branching routines used in a test sequence to describe the steps taken to diagnose a failure successfully.

3.1.173 Diagnostic routine. (1) A logical sequence of tests designed to locate a malfunction of the UUT. (2) The software to perform these tests.

3.1.174 Diagnostic test. (1) A test performed for the purpose of isolating a malfunction in the UUT or confirming that there actually is a malfunction. (2) A test applied to a UUT with the purpose of isolating a fault to a lower level of assembly.

3.1.175 Digital. The use of data carrying signals that are restricted to either of two voltage levels, corresponding to logic "1" or "0".

3.1.176 Digital circuit simulator. A computer program which (upon being fed a description of a digital circuit) simulates the circuit, then (upon generating or being fed test patterns) analyzes how well the patterns exercise (toggle the nodes in) the circuit.

3.1.177 Digital clock. (1) A series of synchronized pulses that determine the bit times (data rate) of a digital pattern. (2) A circuit that generates the synchronized clock.

3.1.178 Digital driver. The output stage of a digital data generator.

3.1.179 Digital section. A portion of ATE that includes all of the digital circuitry required for testing units.

3.1.180 Digital test program comprehension. The ratio between the number of faults capable of being detected by the test program and the total number of faults. This ratio is expressed as a percentage.

3.1.181 Direct memory access. The transfer of data directly from or to computer memory to or from a peripheral.

3.1.182 Don't care state. A portion of primary input or output patterns created for a UUT that are not assigned specific values.

3.1.183 Down time. The period during which a system or device is not operating due to internal failures, scheduled shut down, or servicing.

3.1.184 Driver. (1) An electronic circuit that supplies input to another electronic circuit. (2) A program that exercises a system or system component by

simulating the activity of a higher level component. (3) A program designed for handling communication between the operating system and the specific peripheral device.

3.1.185 Dual port. An architectural implementation which allows ATE hardware resource sharing between two ATE interfaces which may be used for testing different UUTs.

3.1.186 Dummy load. A device or any electronic circuit which provides a simulation of the normal input or output of a circuit or a system under test.

3.1.187 Dynamic dumping. The printing of diagnostic information without stopping the program being tested.

3.1.188 Dynamic functional test. A testing sequence performed at or about rated speed usually done by continuously clocking the UUT.

3.1.189 Dynamic test. A test of one or more of the signal properties or characteristics of an equipment or any of its constituent items performed such that the parameters being observed are measured and assessed with respect to a specified time aperture or response.

3.1.190 Echelon (calibration). A specific level of accuracy of calibration in a series of levels, the highest of which is represented by an accepted national standard. Note: There may be one or more auxiliary levels between two successive echelons.

3.1.191 Edge connector. The portion of a circuit board which is used for communication of input, output and power signals between itself and the prime system.

3.1.192 Electrical partitioning. The electrical or electronic separation of system or unit elements for the purpose of enhanced testing.

3.1.193 Electronic knife. A probe used primarily in digital testing to sense direction of current flow to assist isolation to the defective node in a net.

3.1.194 Embedded test. Test hardware and software which is physically enclosed in the end item or permanently attached to it. Any portion of the system's diagnostic capability that is an integral part of the prime system or support system. 'Integral' implies that the embedded portion is physically enclosed in the prime system or permanently attached - physically or electrically.

3.1.195 End-to-end run time. The end-to-end run time is defined as the time required for a test program to determine that a good UUT is good.

3.1.196 Engineering support data (ESD). Engineering support data consists of text, schematics, drawings, program listings and computer generated outputs, functional flow diagrams, engineering reports (such as Test Strategy Reports (TSRs)) and any relevant technical information to provide for the life cycle support of an end item (end items may be either hard-ware or software end tests).

ESD is required for support at the Depot Level of maintenance, and cognizant field activities.

3.1.197 Entry point. One of a set of points in an ATE program where the test conditions are completely stated and are not dependent on previous tests or setups in any way. Such points are the only ones at which it is permissible to begin part of the complete test program.

3.1.198 Environmental stress screening. Process employing variation of temperature and power used to precipitate/operational defects of a component, board or system before it exits the manufacturing process.

3.1.199 Equipment path measurement. A measurement of the path impedance in a test system, between the UUT and the stimulus source or response monitor.

3.1.200 Equipment replaceable unit. The lowest assembly or individual part that can be fault detected, isolated, removed, replaced and verified to be functional at organizational level without disassembly of the equipment to which it is attached in consonance with the maintenance concept.

3.1.201 Equipment signature. The special characteristics of an equipment's response to a stimulus or of its electrical, electromagnetic, infrared or acoustical emissions.

3.1.202 Equivalent faults. Two or more faults which create the same response for all possible tests. Also referred to as faults, equivalent.

3.1.203 Equivalent gate count. A measure of circuit size. The circuit is analyzed as to its gate structure (NAND, NORS, and so forth) and all gates are counted.

3.1.204 Erasable programmable read only memory (EPROM). A solid-state memory device which, after being programmed, can be reprogrammed. Also known as Electronically Alterable Read Only Memory (EAROM).

3.1.205 Error. The deviation of a computed, observed, or measured quantity from the true, specified or theoretically correct value of the quantity.

3.1.206 Error cone. Refers to the progressive tolerance allowances made at increasingly higher levels of test where components have the tightest tolerance requirements (for example, incoming inspection) progressing to the widest tolerance band at the system level of test (for the same component).

3.1.207 Error-correcting code. A code in which each data signal conforms to specific rules of construction so that departures from this construction in the received signals can be automatically detected, and permits the automatic correction, at the received terminal, or some or all of the errors. Note: Such codes require more signal elements than are necessary to convey the basic information.

3.1.208 Error-detecting code. A code in which each expression conforms to specific rules of construction, so that if certain errors occur in an expression the resulting expression will not conform to the rules of construction and thus the

presence of the errors is detected. Note: Such codes require more signal elements than are necessary to convey the fundamental information.

3.1.209 Error logging. A function of BIT which saves error data (and system status data at the time of the error) in a local storage for the purpose of diagnosing intermittent faults at the next level of maintenance.

3.1.210 Event directed simulation. The simulation of an element when an event occurs on one of its inputs. (An event is the change in a signal value. An element will only change signal value when one or more of its inputs change values. Hence, a given element need only be simulated when an event occurs on one of its inputs).

3.1.211 Exact match fault dictionary. A fault dictionary whose successful utilization is predicated exclusively upon existence of exact matches of observed fault signatures against predicted fault signatures enumerated in the dictionary.

3.1.212 Executable statement. A software statement which will cause some action to be performed during test run-time.

3.1.213 Executive routine. A master set of coded instructions designed to process and control other sets of coded instructions.

3.1.214 Executive test system. A software module which supervises the execution of the test system monitor and module control software.

3.1.215 Exercise. To operate an equipment in such a manner that it performs all its intended functions to allow observation, testing, measurement and diagnosis of its operational condition.

3.1.216 Exercising diagnostics. Routines which exercise the UUT, causin latent and intermittent failures to occur. These are used as a troubleshooting aid.

3.1.217 Expandability. The capability of a system to be increased in capacity or provided with additional functions.

3.1.218 External diagnostics. Any portion of the diagnostic capability that is not embedded.

3.1.219 External test. That portion of a system's testing which does not rely totally on embedded testing resources.

3.1.220 Fail soft. A non-specific deviation in characteristics of a system that has manifested a number of failures but still provides most of its functional capability.

3.1.221 Fail-all simulator. All faults simulated one at a time in serial fashion.

3.1.222 Failed machine response. The output response of a failed UUT when a stimulus is applied.

3.1.223 Failure. Change in operating characteristics of an item resulting in degradation of useful performance.

3.1.224 Failure analysis. Subsequent to a failure, the logical systematic examination of an item, its construction, application, and documentation to identify the failure mode and determine the failure mechanism and its basic cause.

3.1.225 Failure coverage. The ratio of failures detected (by a test program or test procedure) to failure population, expressed as a percentage. Also referred to as percent detect.

3.1.226 Failure criteria. Rules for failure relevancy such as specified limits for the acceptability of an item.

3.1.227 Failure indicator. A device which presents a visual display, audible alarm, or other indication, when a failure or marginal condition exists.

3.1.228 Failure intermittent. Failure for a limited period of time, followed by the item's recovery of its ability to perform within specified limits without any remedial action.

3.1.229 Failure latency. The elapsed time between fault occurrence and failure indication.

3.1.230 Failure mechanism. The physical, chemical, electrical, thermal or other process which results in a failure.

3.1.231 Failure mode. The effect by which a failure is observed to occur.

3.1.232 Failure modes and effects analysis (FMEA). An analysis to identify potential design weaknesses through systematic, documented consideration of the fol-lowing: all likely ways in which a component or equipment can fail; causes for each mode; and the effects of each failure (which may be different for each mission phase).

3.1.233 Failure modes, effects, and criticality analysis (FMECA). A procedure by which each potential failure mode in a system is analyzed to determine the results or effects thereof on the system and to classify each potential failure mode according to its severity.

3.1.234 Failure population. Those failures which are used as a basis for the design and evaluation of tests.

3.1.235 Failure rate. The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated conditions.

3.1.236 Failure universe. The totality of failures possible within a system. Also known as fault universe.

3.1.237 Fall time. The time interval of the pulse trailing edge between the instants at which the instantaneous value first reaches specified upper and lower limits of 90% and 10% of voltage amplitude.

3.1.238 False alarm. A fault indicated by BIT or other monitoring circuitry where no fault exists. Note that a BIT false alarm is actually a malfunction of the BIT.

3.1.239 False alarm rate. (1) The number of false alarms per unit time or other life units (for example, sorties). (2) Number of false alarms per BIT alarms expressed as a percentage.

3.1.240 Fault. (1) A physical condition that causes a device, a component, or an element to fail to perform in a required manner; for example, a short circuit or a broken wire, or an intermittent connection. (2) A degradation in performance due to detuning, maladjustment, misalignment, or failure of parts. (3) Immediate cause of failure (e.g., maladjustment, misalignment, defect, etc.).

3.1.241 Fault class. The grouping of equivalent faults.

3.1.242 Fault collapsing. Faults can be partitioned (collapsed) into classes based upon the concept of dominance and equivalence. Once the faults are partitioned into equivalence classes, only a single representative of each class need be used for both test generation and fault simulation, thus enhancing computational efficiency.

3.1.243 Fault coverage, fault detection, fault comprehension. The ratio of failures detected (by a test program or test procedure) to failure population, expressed as a percentage.

3.1.244 Fault detection. (1) A process which discovers the existence of faults.

3.1.245 Fault dictionary. A list (usually created automatically by an ATPG system) containing each fault signature and the associated failed item (or a group of items) causing the fault signature to be developed by the test program and displayed by the ATE.

3.1.246 Fault dominance. If fault f1 dominates f2, then any test that detects fault f2 also detects fault f1. For example, the output s-a-0 fault of an AND gate dominates any input to that gate s-a-0. Therefore, for the generation of fault detection tests, it is not necessary to consider fault f1.

3.1.247 Fault equivalence. Two or more faults which create the same response for all possible tests.

3.1.248 Fault insertion. (1) Fault insertion, in the context of simulation, is a transformation which maps the original network (the good machine) into a new network (the faulty machine). (2) The process of inserting actual or simulated faults in a UUT for the purpose of demonstrating BIT or test program set (TPS) performance.

3.1.249 Fault intermittent. A failure that occurs and disappears at random without apparent pattern or frequency.

3.1.250 Fault isolated replaceable unit. The replaceable subsystem, assembly, subassembly or component identified through diagnostic testing of a UUT.

3.1.251 Fault isolation. The process of determining the location of a fault to the extent necessary to effect repair.

3.1.252 Fault isolation time. The elapsed time between the detection and isolation of a fault; a component of repair time.

3.1.253 Fault latency time. The extent or duration of time during which the existence of a fault is not known; the elapsed time between fault occurrence and fault indication.

3.1.254 Fault list analysis. Fault simulations is deduced by the propagation of fault lists on nodes of the primitive building block during a single pass simulation. The fault lists are calculated in Boolean arithmetic where the Boolean operators are specified by the primitive building blocks.

3.1.255 Fault localization. (1) The process designed to identify the location of a fault known to exist within a general area of equipment. Fault localization may be less specific than fault isolation. (2) The process of determining the approximate location of a fault.

3.1.256 Fault masking. (1) Equipment design which prevents complete unique fault isolation. (2) A fault X masks a fault Y if no test for fault Y is a test for the faults X and Y occurring jointly in a system.

3.1.257 Fault modes. Fault modes are fault types such as stuck faults, bridging faults, intermittent faults, and functional faults.

3.1.258 Fault resolution. How well the test program (or test procedure) can pin-point the failed item from among other items in the UUT.

3.1.259 Fault resolution, fault isolation. The degree to which a test program or procedure can isolate a fault within an item; generally expressed as the percent of the cases for which the isolation procedure results in a given ambiguity group size. Also known as Fault Isolation Resolution.

3.1.260 Fault signature. The fault signature is the characteristic function of the erroneous response produced by a certain fault.

3.1.261 Fault simulator. A computer program which inserts and studies simulated faults at the nodes of a represented digital circuit being exercised by test stimulus patterns. Also for analog, an analog circuit analysis program which simulates the effect of out-of-tolerance components.

3.1.262 Fault symptom. A measurable or visible abnormality in an equipment parameter.

3.1.263 Fault tolerance. The capacity of a system or program to continue operation in the presence of specified faults.

3.1.264 Feedback. (1) The return of a portion of the output of a circuit or device to its input. (2) A timing signal used as a self-test feature in an automatic test system to verify that a control instruction has been executed before proceeding to the next control instruction.

3.1.265 Feedback Loop. (1) Circuitry returning a portion of its output to its input. (2) A interconnection of faults and signals such that no single test point can successfully isolate the fault location.

3.1.266 Fixed-logic levels. The characteristics of a digital ATE wherein the levels of the digital stimuli provided by the ATE cannot be changed.

3.1.267 Flexible switching. Allows each device in a test system to connect to any pin on the output interfaces.

3.1.268 Foreground or background. (1) The capability to perform two or more tasks concurrently with a computer. (For example, the capability to perform test development tasks concurrent with test execution.) (2) Those effects present in physical apparatus or surrounding environment which limit the measurement or observation of low level signals or phenomenon. Commonly referred to as a noise (background acoustical noise, background electromagnetic radiation, background ionizing radiation).

3.1.269 Forward trace. The process of creating a sensitized path from the failure site to a primary output.

3.1.270 Functional fault. A fault which can be described by a change in the operation of some portion of a system. Also referred to as a fault, functional.

3.1.271 Functional flowchart. A pictorial representation using program-mer symbology to define the sequence of functional testing from initiation through completion.

3.1.272 Functional model. A representative network containing several functional blocks of a unit.

3.1.273 Functional modularity. The splitting of a system into parts or modules based on the function or purpose of these parts.

3.1.274 Functional partitioning. The physical or electrical separation of system or unit elements along interfaces which define and isolate these elements on the basis of function or purpose.

3.1.275 Functional test. (1) A test which determines whether the UUT is functioning properly. The operational environment (such as stimuli and loads) can be either actual or simulated. (2) A test which is intended to exercise an identifiable function of a system. The function is tested independent of the hardware implementing the function.

3.1.276 Functional test flow chart. A chart showing the sequential flow of the functional test sequences making up the total test.

3.1.277 Functional tester. ATE which tests a UUT as a complete, functional entity, typically by applying inputs and sensing outputs only through the UUT's connector(s).

3.1.278 Gate. A logic primitive element, such as an AND, OR, NAND, NOR, exclusive-OR, buffer or invertor device.

3.1.279 Gate level model. A modeling technique in which equivalents for high-level logic elements are constructed from basic gating elements.

3.1.280 General purpose TMDE. Any TMDE that can be used without modification for support operations of more than one end item.

3.1.281 General purpose test equipment. Test equipment which is used for the measurement of a range of parameters common to two or more equipments or systems of basically different design.

3.1.282 General purpose electronic test equipment (GPETE). Electronic test equipment containing the capability without modification, to generate, modify, or measure a range of parameters of electronic functions required to test two, or more prime equipments or systems of basically different design.

3.1.283 Global initialization algorithm. An algorithm that exercises all memory elements of a UUT to their limit.

3.1.284 Gold dot interface adaptor. A type of interface adaptor which uses a system of gold dots to achieve pinless connection. This reduces interface size, increases reliability, eliminates pin alignment problems.

3.1.285 Golden board. A fault-free circuit board used for comparison purposes during testing to identify failed boards. Also referred to as known good board.

3.1.286 Go/no-go test. A set of terms (in colloquial usage) referring to the condition or state of operability of a unit which can only have two parameters: (1) go, functioning properly, or (2) no-go, not functioning properly.

3.1.287 Good machine response. The output response of a failure-free UUT when a stimulus is applied.

3.1.288 GPETE plug-ins. A removable assembly intended to complete or augment the operational capability of a specific item of GPETE (example: oscilloscope preamplifier plug-ins, heterodyne frequency extender plug-ins, digital word generator plug-ins, and so forth).

3.1.289 GPETE support item. The complement of equipment, supplemental to GPETE, which is necessary to facilitate a complete test measurement capability. GSI includes GPETE auxiliary items, GPETE accessories, GPETE plug-ins, and GPETE ancillary equipment.

3.1.290 Gray code. A binary code in which sequential numbers are represented by binary expressions, each of which differs from the preceding expression in one place only.

3.1.291 Ground support equipment. All equipment (implements, tools, test equipment devices -- mobile or fixed -- and so forth) required on the ground to make an aerospace system (aircraft, missile, and so forth) operational in its intended environment.

3.1.292 Ground support equipment recommendation data. A document which reflects a contractor's recommendations for major items of ground support equipment for a specific end item. This document includes identification of testing requirements and is TMDE recommended to satisfy the requirements.

3.1.293 Guarding. A means of connecting an input signal so as to prevent any common-mode signal from causing current to flow in the input, thus differences of source impedance do not cause conversion of the common-mode signal into a differential signal.

3.1.294 Guided probe. An electrical probe to measure status of internal (i.e., between input and output) nodes on a circuit board to perform fault diagnosis. The operator is "guided" by a software algorithm which uses the results of the previous measurement to determine the next node to be measured.

3.1.295 Guided probe system. A fault-isolating technique, in which the test program causes the ATE display to indicate where the test performer should affix the ATE's diagnostic probe on the UUT. The test program then analyzes the signal sensed by the probe and causes the ATE display to indicate where next to affix the probe. This process continues until the fault has been isolated to the best of the test program's capability.

3.1.296 Handshake. (1) An interlocked exchange of signals between a master and a slave, controlling the transfer of data. (2) A hardware or software sequence of events requiring mutual consent of conditions prior to change.

3.1.297 Hard detect. Failures that can be positively detected.

3.1.298 Hard fault. A physical condition that causes a device, component, or element to fail to perform in a required manner; for example, a short-circuit or a broken wire. Also referred to as fault, hard.

3.1.299 Hard line. Any direct electrical connection between the unit under test and the testing device.

3.1.300 Hardware intensive. Applications in which the function is fixed and the application software or firmware is not expected to change or require a redevelopment of the application function itself, should a change be necessary.

3.1.301 Hardwire. To make permanent connections (such as soldered and wire-wrapped connections) between circuits; as contrasted with quick-disconnect connections (such as plug-in, threaded or twist-lock connections).

3.1.302 High order language. A computer language in English terms which represent multiple binary instructions which can be processed directly by the machine (examples: ATLAS, BASIC, and so forth).

3.1.303 Hold. (1) The function of retaining information in one storage device after transferring it to another device. (2) A designed stop in testing. (3) The function of storing information after it has been sampled (for example, sample and hold analog to digital converter).

3.1.304 Horizontal standardization. An item of test equipment used to perform a test function for several different systems.

3.1.305 Hot mockup. Any assemblage of repair parts, components, modules, or similar items configured to simulate an end item or subsystem for the purpose of testing or checking individual or collective parts, components, modules or similar items.

3.1.306 Human interface module. Modules used in the test measurement or diagnostic equipment which provide information exchange between the operator and the machine.

3.1.307 Hybrid circuit. A circuit possessing both digital and analog signals.

3.1.308 Identification test. A test used to verify that the item to be tested is the correct unit.

3.1.309 Impossible detects. Failures which can not be detected by any test sequence due to circuit redundancy or lack of test access.

3.1.310 In-circuit test. Tests of individual components within a circuit while guarding out the effects of surrounding components (analog) or over-riding (digital) inputs.

3.1.311 Independent failure. A failure which occurs without being caused by or related to the failure of associated items, distinguished from dependent failure. Also referred to as failure, independent.

3.1.312 Inherent testability. A measure of testability which is dependent only on item design independent of test stimulus and response data. Inherent testability is a measure of how well the design supports the testing process.

3.1.313 Initial certification only. Certification applied to items of precision measurement equipment (PME) which do not require periodic recalibration. The initial certification is sufficient unless components affecting calibration of the item are replaced.

3.1.314 Initial isolation. Isolation to the equipment/system subunit which must be replaced on line to return the equipment/system to operation. A subunit can be a modular assembly, a printed circuit card which is part of a nonremovable drawer, or a component such as a crystal or antenna subsection. In the event that the maintenance concept requires a subunit to be removed, repaired and then

replaced in the equipment/system, initial isolation includes both isolation to the failed subunit and isolation to the failed removable portion of the subunit.

3.1.315 Initial isolation level of ambiguity. The number of possible equipment/system subunits, as defined above, identified by the Built-in-Test, external test equipment, or manual test procedure, which might contain the failed component. It is possible that a combination of Built-in-Test, external special purpose test equipment, and manual procedures may be necessary to effect isolation. For example, if an equipment test subsystem (Built-in, external, manual) isolates a fault to one of two subunits, the level of ambiguity is equal to two; if it isolates it to one of three subunits the level of ambiguity is equal to three.

3.1.316 Initial value. The value of the output of a system or element just prior to the time a stimulus is applied.

3.1.317 Initialize. To place an item into a known state.

3.1.318 Initiated BIT (IBIT). A subset of BIT which is initiated by some event or the operator; may interrupt normal operation; operator participation may be required. It detects and isolates each fault to the corresponding level of maintenance.

3.1.319 Input. (1) The path through which information is applied to any device. (2) The means for supplying information to a machine. (3) Information transferred from external storage to the internal storage of the machine. (4) The stimuli of a UUT.

3.1.320 Input/Output interface. The connection device in an ATE that has all the analog and digital signals transmitted through it for testing a UUT.

3.1.321 Input fault. A fault at the input terminals of a UUT or components within the UUT. Also referred to as a fault, input.

3.1.322 Input skew. The application of test patterns one at a time to the input contacts of a UUT in order to prevent the ATE's stimulus application method from causing race hazards to occur in the UUT during testing. Also referred to as skew.

3.1.323 Input test vector. A test bit pattern.

3.1.324 Instruction. A set of characters which define an operation, together with one or more addresses (or no address) and which, as a unit, cause the machine to operate accordingly on the indicated quantities. The term "instruction" is preferable to the terms "command" and "order": "command" is reserved for a specific portion of the instruction word or electronic signal; "order" is reserved for the order of the characters (implying sequence) or the order of the interpretation.

3.1.325 Instrument controller. A microprocessor-based programmable machine dedicated to control test equipments through a standardized data bus such as the IEEE 488 GPIB.

3.1.326 Instrumentation. All those devices (chemical, electrical, hydraulic, magnetic, mechanical, optical, pneumatic) utilized to test, observe, measure, monitor, alter, generate, record, calibrate, manage, or control physical properties, movements or other characteristics.

3.1.327 Integrated circuit subroutine. A subroutine in an ATPG computer program. The subroutine simulates the function of a particular integrated circuit.

3.1.328 Integrated diagnostics. A structured process which maximizes the effectiveness of diagnostics by integrating pertinent elements, such as testability, automatic and manual testing, training, maintenance aiding, and technical information as a means for providing a cost effective capability to unambiguously isolate all faults known or expected to occur in weapon systems and equipment and to satisfy weapon system mission requirements. Products of this process are hardware, software, documentation, and trained personnel.

3.1.329 Interface. A shared boundary involving the specification of the interconnection between two equipments or systems. The specification includes the type, quantity and function of the interconnection circuits and the type and form of signals to be interchanged via those circuits.

3.1.330 Interface adapter. An item providing electronic, electrical and mechanical compatibility between the UUT and the test equipment. Also referred to as a test adapter.

3.1.331 Interface controller. A device which enables a computer to transmit and receive digital information for programming an instrument or peripheral.

3.1.332 Interface device (ID). The ID is any device which provides mechanical and electrical connection and signal conditioning between the test equipment and the UUT. The ID may also provide signal conditioning.

3.1.333 Interface testing. Testing conducted to ensure that program or system components pass information or control correctly to one another.

3.1.334 Intermediate frequency. A frequency to which a signal is shifted locally as an intermediate step in transmission or reception.

3.1.335 Intermediate maintenance. Maintenance which is the responsibility of and performed by designated maintenance activities for direct support of the using organizations. Its phases normally consist of cali-bration, repair or replacement of damaged or unserviceable parts, components or assemblies; the emergency manufacture of non-available parts and providing technical assistance to using organizations.

3.1.336 Intermittent failure. A failure that occurs and disappears at random without apparent pattern or frequency. Also referred to as failure, intermittent.

3.1.337 Internal fault. A fault internal to an integrated component or device such as an integrated circuit. Also referred to as a fault, internal.

3.1.338 Interoperability. (1) The ability of systems, units or forces to provide services to and accept services from other systems, units or forces and to use the services so exchanged to enable them to operate effectively together. (2) The condition achieved among communication-electronics equipment when information or services can be exchanged directly and satisfactorily between them and their users. The degree of interoperability should be defined when referring to specific cases.

3.1.339 Inverted-pyramid. The specification of tighter test tolerances at the factory (or at component or subassembly indenture levels) which gradually loosen at succes-sive maintenance levels (or higher assembly indenture levels, system level being the highest.) Also known as inverted pyramid. The use of a cone of tolerance approach tends to reduce RTOK problems.

3.1.340 Item. A nonspecific term used to denote any unit or product including materials, parts, subassemblies, equipments, accessories or part.

3.1.341 Iterative. Describing a procedure or process which repeatedly executes a series of operations until some condition is satisfied. An iterative procedure may be implemented by a loop in a routine.

3.1.342 Knowledge based test. A test based in part on previously acquired and stored information.

3.1.343 Known good board. A fault-free circuit board. Also referred to as Golden board.

3.1.344 Laboratory reference standards. Standards that are used to assign and check the values of laboratory secondary standards.

3.1.345 Laboratory secondary standards. Standards that are used in the routine calibration tasks of the laboratory.

3.1.346 Laboratory working standards. Those standards that are used for the ordinary calibration work of the standardizing laboratory. Note: Laboratory working standards are calibrated by comparison with secondary standards of that laboratory.

3.1.347 Learn mode testing. The utilization of random test patterns as stimuli for a circuit to produce a change in state at the output.

3.1.348 Level of repair analysis. A technique which establishes whether an item should be repaired or discarded; and at what maintenance level, that is, organizational, intermediate, or depot it should be repaired.

3.1.349 Limit. The extreme of the designated range through which the measured value of characteristics may vary and still be considered acceptable.

3.1.350 Line replaceable unit (LRU). A unit designated to be removed upon failure from a larger entity (equipment, system) in the operational environment.

3.1.351 Linearity. The condition wherein the change in the value of one quantity is directly proportional to the change in the value of another quantity.

3.1.352 Load. (1) To read information from cards, disc or tape into memory. (2) Building block or adapter providing a simulation of the normal termination characteristics of a UUT. (3) The effect that the test equipment has on UUT or vice versa.

3.1.353 Loading error. (1) An error due to the effect of a load upon the transducer or signal source driving it. (2) The error introduced when data are incorrectly transferred from one medium to another.

3.1.354 Local pin storage. Digital data stored in a memory element such as a shift register or random access memory (RAM) for each pin in a digital device used for clocking out data or reading in data at a predetermined rate.

3.1.355 Logic diagram. (1) A diagram representing the logic elements and their interconnections without necessarily expressing construction or engineering details. (2) A diagram that depicts the two-state device implementation of logic functions with logic symbols and supplementary notations, showing details of signal flow and control, but not necessarily the point-to-point wiring.

3.1.356 Logic simulation. The process of building and exercising a model of a digital circuit on a computer. The function of a logic simulator is to compute signal values as a function of a logic simulator is to compute signal values as a function of time in an arbitrary circuit, given the initial state and input sequence to the circuit.

3.1.357 Logic value. A digital value of "1" or "0" (high or low state).

3.1.358 Low speed digital. Generating and receiving digital data at the computer recycle rate.

3.1.359 Lowest replaceable unit (LRU). The lowest unit designated to be removed upon failure from a larger entity (equipment, system).

3.1.360 Maintainability. The measure of the ability of an item to be retained in or restored to specified condition when maintenance is performed by personnel having specified skill levels, using prescribed procedures and resources, at each prescribed level of maintenance and repair.

3.1.361 Maintainability, mission. The measure of the ability of an item to be retained in or restored to specified condition when maintenance is per-formed during the course of a specified mission profile. (The mission-related system maintainability parameter).

3.1.362 Maintenance. Activity intended to keep equipment (hardware) or programs (software) in satisfactory working condition, including tests, measurements, replacements, adjustments, repairs, program copying, and program improvement. Maintenance is either preventive or corrective.

3.1.363 Maintenance aid. A device or guide used on the job to facilitate performance of maintenance.

3.1.364 Maintenance concept. A description of the general scheme for maintenance and support of an item in the operational environment.

3.1.365 Maintenance engineering analysis. A process performed during the development stage to derive the required maintenance resources such as personnel, technical data, support equipment, repair parts, and facilities.

3.1.366 Maintenance level. The level at which maintenance is to be accomplished, that is, organizational, intermediate, and depot.

3.1.367 Malfunction. (1) A physical condition that causes a device, a component, or an element to fail to perform in a required manner; for example, a short or open circuit or an intermittent connection. (2) A degradation in performance due to detuning, maladjustment, misalignment, or failure of parts. (3) Immediate cause of failure (e.g., maladjustment, misalignment, defect, etc.).

3.1.368 Manual checkout. A checkout system which relies completely on manual operation, operator decision and evaluation of results.

3.1.369 Manual procedures. Any procedure which requires (1) measurements using general purpose test equipment, or (2) a series (more than one) of sequential remove and replace actions on subunits (subunit component/parts), (lowest level replacements internal to subunit components/parts), some of which are non-failed, in order to diagnose and isolate a failed subunit (subunit component/part), (lowest level replacement internal to a subunit component/part).

3.1.370 Manual test equipment. A system or device used to test end items or subsystems which relies primarily on manual opera-tion and operator evaluation of results.

3.1.371 Marginal checking. A system or method of determining circuit weaknesses and incipient malfunctions by checking specific operating characteristics such as leakage current, electromagnetic or thermal properties, voltage levels, etc., or by varying the operating conditions of the circuitry.

3.1.372 Marginal testing. Testing the current results on an indicator that has tolerance bands for evaluating the signal or characteristics being tested. (For example: a green band might indicate an acceptable tolerance range representing marginal operation: and a red band, a tolerance that is unsatisfactory for operation of the item).

3.1.373 Mask file. A file which is used to determine which measured values at a particular test step are valid or invalid.

3.1.374 Master test program set index. A reference system keyed by UUT identifier that contains a part number description of all the TPS elements needed to execute a test program.

3.1.375 Mean time between failures (MTBF). A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

3.1.376 Mean time to repair (MTTR). A basic measure of maintainability: The sum of corrective maintenance times at any specific level of repair, divided by the total number of failures within an item repaired at that level, during a particular interval under stated conditions.

3.1.377 Measurement. The determination of the magnitude or amount of a quantity by comparison (direct or indirect) with the prototype standards of the system of units employed.

3.1.378 Measurement range. That part of the total range within which the requirements for accuracy are to be met.

3.1.379 Measurement standard. A measuring instrument or artifact used as reference to establish and maintain the accuracy of other measuring instruments or artifacts. Measurement standards may be used to calibrate other standards of lesser accuracy or to calibrate test and measurement equipment directly.

3.1.380 Measurement uncertainty. The limits of error about a measured value between which the true value will lie with the confidence stated.

3.1.381 Memory cycle. The time required to read information from memory and replace it.

3.1.382 Metrology. The science of measurement for determination of conformance to technical requirements including the development of standards and systems for absolute and relative measurements.

3.1.383 Microelectronics. Microelectronics is that area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

3.1.384 Minimum access code. A system which minimizes the effect of delays for transfer of data or instructions between storage and other machine units.

3.1.385 Mission equipment. Any item which is a functional part of a system or subsystem and is required to perform mission operations.

3.1.386 Mission profile. A time-phased description of the events and environments an item experiences from initiation to completion of a specified mission, to include the criteria of mission success or critical failures.

3.1.387 Mnemonic. Assisting or intending to assist a human memory and understanding. Thus a mnemonic term is usually an abbreviation, that is easy to remember: for example, mpy for multiply and acc for accumulator.

3.1.388 Mnemonic code. A pseudo code in which information, usually instructions, is represented by symbols or characters which are readily identified with the information.

3.1.389 Mode code. A means by which the bus controller can communicate with the multiplex bus related hardware, in order to assist in the management of information flow.

3.1.390 Modeling. Modeling is the process of describing a circuit (schematic) in terms of the primitives of the processing system such that the result from the simulator will correspond to the signal values in the actual circuit.

3.1.391 Modular software. A program structure implemented as independent functional sections to preclude extensive housekeeping in the accommodation of changes.

3.1.392 Modularity (software). The extent to which software is composed of discrete components such that a change to one component has minimal impact on the other components.

3.1.393 Module. A component, or a complete subassembly combined in a single package, that is designed to be removed and replaced easily for main-tenance or repair.

3.1.394 Monitor. To check and measure selected parameters of an operating system.

3.1.395 Moving element. Those parts that move as a direct result of a variation in the quantity that the instrument is measuring. Note: (1) The weight of the moving element includes one-half the weight of the springs, if any. (2) The use of the term movement is deprecated.

3.1.396 Multiplexer. An electronic multiposition switch that allows for the selection of any one of number of signals.

3.1.397 Multiport ATE. An ATE system which contains more than two functional interfaces and shares a common set of test resources.

3.1.398 Negative test. A test for which the proper response to a stimuli is no response, such as a command deliberately formatted with a syntax error to check the accept or reject circuitry.

3.1.399 Net. A group of I/O nodes connected together.

3.1.400 Nibble. A four bit byte.

3.1.401 Node. (1) One of the set of discrete points in a flow graph. (2) An end point of any branch of a network or graph, or a junction common to two or more branches. (3) In a network, a point where one or more functional units interconnect transmission lines.

3.1.402 Nominal delay. The time the signals take to propagate through a logic element or even a wire. The effect of an input change to an element on the output will not occur until after the duration of nominal delay.

3.1.403 Noncritical failure. Any failure which degrades a performance or results in degraded operation requiring special operating techniques or alternative modes of operation which could be tolerated throughout a mission, but should be corrected immediately upon completion of mission. Also referred to as a failure, noncritical.

3.1.404 Nondestructive testing. Testing of a nature which does not impair the usability of the item.

3.1.405 Nondetectable fault. A fault which cannot be detected (usually with reference to a particular test program set or set of test patterns). Also referred to as a fault, nondetectable.

3.1.406 Noninterference testing. A type of on-line testing that may be carried out during normal operation of the unit under test without affecting the operation.

3.1.407 Nonrelevant failure. (1) A failure verified as having been caused by a condition not present in the operational environment. (2) A failure veri-fied as peculiar to an item design that will not enter the operational inventory. (3) A failure which will not be included in interpreting test results or in cal-culating the value of a reliability characteristic. Also referred to as failure, nonrelevant.

3.1.408 Nonrepairable subassembly. A component, module, or subassembly is nonrepairable if the physical nature of the item is such that the item cannot be economically or feasibly repaired due to the excessive cost of material and labor required to effect such repair. This excessive cost is normally considered as 65 percent, or greater, of the acquisition cost of the item. (Examples of nonre-pairable subassemblies are: (a) an integrated circuit, (b) an encapsulated printed circuit card wherein the components and card are sealed in a hard ther-mosetting plastic compound, and (c) a module wherein all printed circuit cards or components are sealed in a hard thermosetting plastic compound or the module is hermetically sealed).

3.1.409 Normal mode noise. A combination of residual common mode noise and induced system noise.

3.1.410 Normal mode noise rejection. The inherent ability of an instrument to integrate a signal, thereby averaging out and reducing the effective normal mode noise.

3.1.411 Normalize. (1) To adjust the characteristics and fraction of a floating decimal point number thus eliminating leading zeros in the fraction. (2) To adjust a measured parameter to a value acceptable to an instrument or measurement technique.

3.1.412 Null. The condition of minimum output of a circuit as a function of some adjusting device.

3.1.413 Null balance. The condition that exists in the circuits of an instrument when the difference between an opposing electrical quantity within the instrument and the measured signal does not exceed the dead band. Note: The value of the opposing electrical quantity produced within the instrument is related to the position of the end device.

3.1.414 Observability. An attribute of equipment design which defines or describes the extent to which signals of interest may be observed.

3.1.415 Off-line test equipment. Equipment used to perform tests on a UUT with the item removed from its normal operating environment.

3.1.416 Off-line testing. The testing of a UUT with the item removed form its normal operational environment.

3.1.417 On-line calibration. Calibration of ATE hardware through the use of existing ATE assets which can be certified as: (1) within specified tolerance limits; (2) providing test accuracy ratios of at least 4:1.

3.1.418 On-line test equipment. Equipment used to perform tests on a UUT while the item is in its normal operating environment.

3.1.419 On-line testing. The testing of the UUT in its operational environment.

3.1.420 On-off test. A test conducted by repeatedly switching on and off either the signal, power, or lead connected to the UUT while observing the reaction or performance of some parameter of that UUT. A test frequently use to isolate offending equipment while conducting compatibility, interference, or system evaluations.

3.1.421 Open fault. A fault caused by an electrical separation of normal electronically-connected points. Also referred to as a fault, open.

3.1.422 Operable. The state of being able to perform the intended function.

3.1.423 Operable equipment. An equipment which, from its most recent performance history and a cursory electrical and mechanical examination, displays an indication of operational performance for all required functions.

3.1.424 Operational assurance, fault isolation. Self-test program used on ATE.

3.1.425 Operational suitability. The degree to which a system can be satisfactorily operated in the field, with consideration being given to availability, safety, human factors, electromagnetic compatibility, logistic supportability, and training requirements.

3.1.426 Operational test program (OTP). The test program for a specific UUT or functionally related group of UUTs, in a medium designed for field use with the applicable ATE or TMDE, or both.

3.1.427 Operational test program set (OTPS). The OTPS shall be a single TPS or a group of TPSs consisting of those items of hardware, software and documentation which enable the Unit Under Test (UUT) to be connected to, test, fault detect and fault isolate to a failed SRA and/or component and verify repairs utilizing an ATE system. The OTPS shall be the result of merging one or more TPSs into a group which share a single ID for testing a selected grouping of Weapon Replaceable Assemblies (WRAs) or Shop Replaceable Assemblies (SRAs) on an ATE system. The Interface Device (ID) TPS is part of the OTPS. The OTPS shall consist of an Operational Test Program Medium (OTPM), an Operational Test Program Instruction (OTPI), Operational Test Program Hardware (OTPH), and the Master Test Program Set Index (MTPSI) deck.

3.1.428 Organizational maintenance. Maintenance which is the responsibility of and performed by using organizations on its assigned equipment. Its phases normally consist of inspecting, servicing, lubricating, adjusting and the replacing of parts, minor assemblies and subassemblies.

3.1.429 Oscillation control. Oscillation control is a mechanism in simulators to inhibit potential and real oscillation which creates high circuit activity by limiting the number of times a signal line can change. A line which changes more than the preset number of times is set to the unknown state. Eventually, the circuit will stabilize with every line that was involved in the oscillating loop set to the unknown state.

3.1.430 OTP instruction. The OTP instruction provides information need for testing (e.g., hook-up, probe point locations or other programmed operator intervention) which cannot be conveniently provided by the ATE under control of the OTP. Appropriate contents are largely dependent on the ATE being used.

3.1.431 Out-of-tolerance fault. A defect or malfunction in a component, assembly or system in which a performance parameter approximates but falls outside the prescribed upper or lower limit for the parameter. Also referred to as a fault, out-of-tolerance.

3.1.432 Output. (1) Current, voltage, power, pressure, flow, or any other driving force delivered by a circuit or device. (2) Terminals or other places where current, voltage, power, pressure, flow, or any other driving force may be delivered by a circuit or device. (3) In computers, information transferred from internal storage to external storage or other peripheral equipment.

3.1.433 Output termination. To terminate the output of a UUT (such as a radio transmitter or receiver) with a dummy load to simulate its normal operating environment.

3.1.434 Output test vector. An ordered set of simultaneously observed output values.

3.1.435 Over-range. An input to a measuring device which exceeds in magnitude the capability of the selected range of that device.

3.1.436 Overshoot. The amount by which a pulse amplitude exceeds some set reference value after it has changed its state. Also, considered a distortion which occurs after a major pulse transition.

3.1.437 Parallel fault simulation. The simultaneous simulation of two or more faults by the fault simulation program in an ATPG system.

3.1.438 Parallel simulation. Since a word computer memory consists of many bits, several failures can be simulated simultaneously through a fault insertion mechanism. This is possible because logic instructions on a computer maintain the independence of different bits in a word.

3.1.439 Parameter. (1) Any specific quantity or value affecting or describing the theoretical or measurable characteristics of a unit being considered which behaves as an independent variable or which depends upon some functional interaction of other quantities in a theoretically determinable manner: and (2) In programming, a variable that is given a constant value for a specific purpose or process.

3.1.440 Parametric fault. A fault which causes some parameters for device to have a value outside its specified range.

3.1.441 Parametric testing. Testing a UUT's ability to function correctly within acceptable tolerance testing when all parameters (for example, power supply voltages) are varied within specified limits.

3.1.442 Parity BIT. A binary digit appended to an array of bits to make the sum of all the bits always odd or always even.

3.1.443 Parity check. A summation check in which the bits in a character or block are added (module 2) and the sum checked against a single, previously computed parity digit: that is, a check that test whether the number of ones is odd or even.

3.1.444 Partial failure. Failure resulting from deviation in characteristics beyond specified limits but not sufficient to cause a complete lack of function. Also referred to as a failure, partial.

3.1.445 Partition. To divide circuitry into easy-to-test sections.

3.1.446 Partitioning. The physical, functional or electrical separation of system or unit elements.

3.1.447 Passive BIT. A type of BIT which is non-disruptive and noninterfering to the prime system. Also referred to as BIT, passive.

3.1.448 Passive sensor. (1) A sensor requiring no source of power other than the signal being measured. (2) A sensor that provides a signal after being stimulated by the UUT.

3.1.449 Passive test. A test conducted upon an un-energized UUT (also called cold test).

3.1.450 Patchboard. A device composed of a board containing a matrix of electrical terminals into which short interconnecting cables (patchcords) may be plugged in patterns to establish a selected circuit configuration for specific programs. To change the circuit configuration, one wired-up patchboard is removed and another wired-up patchboard is inserted.

3.1.451 Patchcord. An interconnecting cable for plugging or patching between terminals; commonly employed on patchboard, plugboard, and in maintenance operations.

3.1.452 Path sensitization. A process of creating a sensitized output path for fault-dependent test program generation.

3.1.453 Pattern generator. A procedure which generates input stimuli for a circuit. Pattern generators are divided into two groups, fault independent procedures such as random number generators and fault dependent strategies such as path sensitization algorithms.

3.1.454 Pattern sensitive failure. A component failure, usually internal to the component, whose effect at the component's output pin(s) is dependent upon the input applied.

3.1.455 Peculiar support equipment. Support equipment which is compatible with only one item.

3.1.456 Percent detect. The ratio of failures detected (by a test program or test procedure) to failure population, expressed as a percentage. Also referred to as failure coverage.

3.1.457 Performance monitoring. A process of continuously or periodically scanning a selected number of test points on a non-interfering basis to determine if the unit is operating within specified limits.

3.1.458 Performance test. A test which verifies if the UUT is performing properly.

3.1.459 Performance verification. Performance testing monitored by Government personnel to verify proper performance.

3.1.460 Periodic BIT. A type of BIT which is initiated at some regular interval. An example of BIT software executing during planned processor idle time. Also referred to as BIT, periodic.

3.1.461 Periodic check. A test or series of tests performed at designated intervals to determine if all elements of the UUT or test system are operating within their designated limits.

3.1.462 Personality card. A printed circuit card which is inserted in a test adapter to make the test adapter compatible with I/O personality of a particular UUT.

3.1.463 Pickoff. A device that senses change to create a signal or to effect some type of control.

3.1.464 Pinboard. A programming or switching device composed of a removable or semipermanent board containing a matrix of holes or jacks into which short pins may be placed in patterns to establish a circuit configuration for specific programs or tests.

3.1.465 Pin electronics. An ATE architectural implementation to minimize system performance degradation due to cabling and interface constraints by including full test capability at each interface pin.

3.1.466 Pipeline processing. Pipeline processing refers to a simulation technique which allows new input vectors to be applied to a modeled circuit before the circuit has stabilized from the last input vector. This simulation technique is valuable when used in conjunction with dynamic test which can exercise UUT's at their operating speeds typically in excess of 1 mega-hertz. Pipeline processing simulators usually employ a real time concept rather than an arbitrary unit time.

3.1.467 Plugboard. The same as patchboard but use is restricted to punched card machines.

3.1.468 Portability. (1) The ability of test procedures to be used by more than one test equipment configuration. (2) The ease with which software can be transferred form one computer system or environment to another.

3.1.469 Portable equipment. Portable equipment is designed to be easily carried between locations of use. Equipment of 5 kg (11 lbs), or less in weight which is readily hand held with no handle(s), or 20 kg (44 lbs), or less, and provided with a handle(s), shall be considered to be portable. In MIL-STD-28800, portable equipment may be of Style A, C, or D, but include some Style E equipment designed for portable as well as bench top use.

3.1.470 Possible detect. A possible detect results when the unknown or indeterminate bits of a failed UUT response constitute the only difference from the response of a good UUT.

3.1.471 Post processor. (1) A set of computer instructions that transform tool centerline data into machine motion commands using the proper tape code and format required by a specific machine/control system. Instructions such as feedrate calculations, spindle-speed calculations, and auxiliary-function commands may be included. (2) A software tool which converts the output of a simulator into ATE source code.

3.1.472 Postmortem. A routine that causes the information concerning the contents of all internal registers and storage locations to be printed in order to locate a mistake.

3.1.473 Potential fault detection. Same as fault detection except the outputs are in such a way that the good output is 0 or 1 while the fault output is X (unknown).

3.1.474 Power or stimuli short test. A power or stimulus input check made to verify that the input is not operating into a short circuit.

3.1.475 Power-on BIT (PBIT). A subset of BIT which is initiated when subsystem electrical power is turned on and terminates before equipment is ready for normal operation. It is an automatic one-time test sequence that detects and isolates each fault to the corresponding level of maintenance.

3.1.476 Precision. A measure of consistency or repeatability of a set of measurements.

3.1.477 Precision measurement equipment (PME). Test and measurement equipment used to measure, calibrate, gauge, test, inspect, diagnose, or otherwise examine material, supplies, and equipment to determine whether they comply with the established specifications.

3.1.478 Preemptive control. An action or function which, by reason of preestablished priority, is able to seize or interrupt the process in progress and perform a process of higher priority.

3.1.479 Preferred items list. A listing of equipment which denotes the equipment considered the most advanced and acceptable, in its family, for military use.

3.1.480 Presence tests. Actions which verify the presence or absence of signals or characteristics. Such signals or characteristics are those which are not critical to the operating of the item within its tolerances.

3.1.481 Preshoot. A distortion which occurs prior to a major pulse transition.

3.1.482 Primary failure. A failure which occurs without being related to the failure of associated items, distinguished for dependent failure.

3.1.483 Primary I/O. The pins or connections of the UUT which provide only the power or signals necessary for proper operation.

3.1.484 Primitive model. The description of a UUT by primitives. It is actually a microfunctional model, which is one level higher than the gate-level model.

3.1.485 Primitive. The basic blocks or operators used by a simulation system, whose inputs and outputs are binary valued, and for which the signal propagational delay characteristics through the device can be specified. There are several levels of primitives used by different simulation systems. Some systems use combinational gates and Boolean operators only. Other systems include sequential elements such as latches, flip-flops, delay lines, and monostable in their primitive sets. Some systems consider counters, shift registers, ROM and RAM

as primitives. Primitives are not expanded into equivalent circuits but are handled as single blocks by interpretive subroutines.

3.1.486 Printed circuit board. A board provided for mounting of electrical components on which most connections are made by conductive circuit paths printed on the board.

3.1.487 Probable fault. A hard or soft fault that is most likely to occur, relative to all possible faults within the UUT. A component having a high failure rate. Also referred to as a fault, probable.

3.1.488 Production acceptance test. Production acceptance testing is a test, inspection and quality assurance process used to ascertain that production units of material are in conformance with production specifications (and, usually, the verified first article.)

3.1.489 Prognostics. The use of test, performance, or other related data in the evaluation of a system or equipment for determining the potential of impending faults.

3.1.490 Programmable driver. A driver which insures (through programmability of voltage levels) compatibility with multi-logic families.

3.1.491 Programmable instrumentation. Test instruments that can be controlled automatically by an external device.

3.1.492 Programmable stimuli. Stimuli that can be controlled in accordance with instructions from a controlling device.

3.1.493 Programmable stimuli-generating instrument. An instrument whose stimuli-generating functions can be automatically controlled.

3.1.494 Programmer-comparator. A device which (1) reads commands and data form a sequential program usually on tape or cards. (2) Sets up delays, switching, stimuli, and performs measurements as directed by the program. (3) Compares the results of each measurement with fixed programmed tolerance limits to arrive at a decision.

3.1.495 Pseudo-instruction. An instruction which resembles the instructions acceptable to the computer but which must be translated into actual computer instructions in order to control the computer.

3.1.496 Pseudo-random patterns. A repeatable sequence of digital patterns that has the appearance of being random.

3.1.497 Quality assurance. Planned and systematic actions necessary to provide adequate confidence that a system or component will perform satisfactorily in service.

3.1.498 Quality assurance software. Computer programs used to test cases, simulators, validation and verification tools to certify the quality of operation or test computer programs.

3.1.499 Quantitative testing. Testing that monitors or measures the specific quantity, level or amplitude of a characteristic to evaluate the operation of an item. The outputs of such tests are presented as finite or quantitative values of the associated characteristics.

3.1.500 Quieting sensitivity. The level of a continuous wave input signal which will reduce the noise output level of a frequency modulation receiver by a specified amount, usually 20 decibels.

3.1.501 Race hazard. Close or simultaneous timing between signals that can result in erratic circuit operation.

3.1.502 Rack. A framework, constructed of rails or structural members, for mounting an assembly of modules for monitoring, measuring, and controlling remotely operated systems.

3.1.503 Rack and stack. An ATE which relies on system integration of applicable units of test equipment.

3.1.504 Random access. Selection of any test point without regard to a fixed sequence.

3.1.505 Random failure. Any failure whose occurrence is unpredictable in an absolute sense but which is predictable only in a probabilistic or statistical sense. Also referred to as a failure, random.

3.1.506 Range. (1) (Instrument) -- The range of values within which a measuring instrument is capable of measuring or which a generating instrument is capable of generating. (2) (Computing System) -- (a) The set of values that a quantity or function may assume. (b) The difference between the highest and the lowest values that a function may assume.

3.1.507 Rapid access loop. Internal memory machines in which a small section of memory has much faster accessibility than the remainder of the memory.

3.1.508 Rated accuracy. The limit that errors will not exceed when the instrument is used under any combination of rated operating conditions. Note: (a) It is usually expressed as a percent of the span. It is preferred that a + sign or - sign or both precede the number or quantity. The absence of a sign infers a $\pm$ sign. (b) Rated accuracy does not include accuracy of sensing elements or intermediate means external to the instrument.

3.1.509 Rated operating conditions. The limits of specified variables or conditions within which the performance ratings apply.

3.1.510 Readiness test. A test specifically designed to determine whether an equipment or system is operationally suitable for a mission.

3.1.511 Readout. (1) The device used to present output information to the operator, either in real time or as an output of a storage medium. (2) The act of reading, transmitting, displaying information either in real time or from an

internal storage medium of an operator or an external storage medium or peripheral equipment.

3.1.512 Real time testing. Testing the UUT at its normal operating frequency and timing.

3.1.513 Recovery time. The time required for a signal to return to its rated value after a sudden change.

3.1.514 Redundancy. In an item, the existence of more than one means for performing a given function.

3.1.515 Redundant design. Alternate or parallel methods of performing a given function that are not necessary for system operation but are utilized when the primary function fails.

3.1.516 Reference conditions. The values assigned for the different influence quantities at which or within which the instrument complies with the requirements concerning errors in indication.

3.1.517 Reference quantity. A selected value of a parameter from which departure of similar parameters is measured.

3.1.518 Reference standards. Standards (that is, primary, secondary and working standards, where appropriate) used in a calibration program. These standards establish the basic accuracy limits for that program.

3.1.519 Relevant failure. Failure to be included in interpreting test results or in calculating the value of a reliability characteristic. Also referred to as a failure, relevant.

3.1.520 Reliability. (1) The probability of failure-free performance for a specified interval under stated conditions. (2) The probability that an item can perform its intended function for a specified interval understated conditions. (For non-redundant items this is equivalent to definition (1). For redundant items this is equivalent to definition of mission reliability).

3.1.521 Repairable item. An item which can be restored to perform all of its required functions by corrective maintenance.

3.1.522 Repeatability. The closeness of agreement among repeated measurements of the same variable under the same conditions.

3.1.523 Replaceable module. An item that is designed and packaged in an replaceable unit for ready removal and replacement.

3.1.524 Replaceable unit. Any unit that is designed and packaged to be readily removed and replaced in an equipment system without unnecessary calibration or adjustment.

3.1.525 Reserve. The setting aside of a specific portion of memory for storage area.

3.1.526 Reset. (1) To restore a register, counter or flip-flop to an initial state. (2) To initialize a system or test system.

3.1.527 Residual frequency modulation. A measure of short term stability of an oscillator or synthesizer output and is usually expressed in hertz peak to peak.

3.1.528 Resolution. The least value of the measured quantity which can be distinguished.

3.1.529 Response. The reaction of a device to a stimulus.

3.1.530 Response time. The time required for a resulting condition to reach the steady state after variation of an input quantity.

3.1.531 Re-test OK (RTOK). A unit that was identified as malfunctioning in a particular manner at one maintenance level, but that specific malfunction could not be duplicated at a higher maintenance level facility.

3.1.532 Rise time. The time interval of the leading edge between the instants at which the instantaneous value first reached the specified lower and upper limits (10 percent and 90 percent) of programmed or fixed output amplitude.

3.1.533 Round off. To the least-significant digit or digits of a numeral and to adjust the part retained in accordance with some rule.

3.1.534 Rounding. A distortion appearing as a rounded feature and occurring at a point where a change of slope is expected or described.

3.1.535 Rounding error. The error resulting from deleting the less significant digits of a quantity and applying some rule of correction to the part retained. A common roundoff rule is to take the quantity to the nearest digit. Thus the value of Pi, 3.14159265..., rounded to four decimals is 3.1416.

3.1.536 Run time performance verification. A software routine usually associated with third generation ATE which provides software adjustments of stimulus and response prior to test execution to assure test accuracy.

3.1.537 Run time variable. An application program condition in which the stimuli is varied under system control based on a measurement result.

3.1.538 Schematic. A diagram which shows a symbol for each part in the system and shows the connections between components. The part symbols are arranged in order of signal/process flow.

3.1.539 Screening test. A test, or combination of tests, intended to remove unsatisfactory items or those likely to exhibit early failures.

3.1.540 Secondary failure. A non-specific condition of a system that has manifested a number of failures but still provides most of its functional capability. Also referred to as a failure, secondary.

3.1.541 Secondary isolation. Isolation to the subunit component/part which must be replaced in the shop to return the subunit to serviceable condition. The subunit component/part can be modular assembly, a printed circuit card, or a piece part. In the event that Initial Isolation Level of Ambiguity necessitates the removal and replacement of two or more subunits (only one of which has malfunctioned) Secondary Isolation includes both isolation to the actual failed subunit (after removal from the system/ equipment) and isolation to the component/part in the failed subunit.

3.1.542 Secondary isolation level of ambiguity. The number of possible subunit components/parts as defined above, identified by Built-in-Test, external tester or manual test procedures, which might contain the failed component/part (it is possible that a combination of Built-in-Test, external testers, and manual procedures might be necessary to effect isolation). For example, if a subunit test system (say a tester) isolates the faulty component to one of two printed circuit cards the level of ambiguity is two, if it isolates to one of three printed circuit cards the level of ambiguity is equal to three.

3.1.543 Segment. Those portions of a computer program or test program that must be broken down or segmented due to size limitation of a computer's memory.

3.1.544 Self-test. A self-test is a test or series of tests, performed by a device upon itself, which shows whether or not it is operating within designed limits. This includes test programs on computers and ATE which check out their performance status and readiness.

3.1.545 Self-test adapter. An item used to replace the UUT during the self-test of an ATE.

3.1.546 Self-test capability. Self-test capability is the ability of a device to check its own circuitry and operation. The degree of self-test is dependent on the ability to detect and possibly isolate a fault.

3.1.547 Semi-automatic self-test. Self-test which, in order to achieve a higher level of accuracy or fault isolation than that achievable by automatic self test, requires human intervention to reach inaccessible test points or to employ external test equipment or standards, or both.

3.1.548 Semi-automatic test equipment. Any automatic testing device which requires human participation in the decision making control, or evaluative functions.

3.1.549 Sensitivity. The ratio of the magnitude of its response to the magnitude of the quantity measurement.

3.1.550 Sensitized path. A signal path conditioned so that a designated signal may propagate, unaffected by other states, to a primary output.

3.1.551 Sensor. A device that responds to a physical stimulus (such as heat, light, sound, pressure, magnetism, or motion) and transmits a resulting electrical signal for measurement or control.

3.1.552 Sequential logic. Digital circuits whose subsequent behavior depends on specific sequences of events that have occurred earlier.

3.1.553 Serial simulator. Fault simulation is done with only one fault inserted in the circuit. The simulator simulates it over the entire stimuli set. The process is repeated for all faults.

3.1.554 Service routine. A routine in general support of the operation of a programmable machine (for example, an I/O diagnostic, tracing, or monitoring routine). Synonymous with utility routine.

3.1.555 Service test. A test of an item, system, material or technique conducted under simulated or actual operational conditions to determine whether the specified requirements or characteristics are satisfied.

3.1.556 Shop replaceable assembly (SRA). An item which is designated to be removed or replaced upon failure from a higher level assembly in the shop (intermediate or depot maintenance activity), and is to be tested as a separate entity. Also referred to as a shop replaceable unit.

3.1.557 Shop replaceable unit (SRU). An item that is designated to be removed or replaced upon failure from a higher level assembly in the shop (intermediate or depot maintenance activity) and is to be tested as a separate entity. Also referred to as a shop replaceable assembly.

3.1.558 Signature analysis. A digital test approach which uses circuit-generated stimulus and synchronization and compresses the response data into a compact signature.

3.1.559 Signature diagnosis. The examination of the electronic signature of an equipment for deviation from known or expected characteristics and consequent determination of the nature and location of malfunctions.

3.1.560 Significance. The value or weight given to a position, or to a digit in a position, in a positional numeration system. In most positional numeration systems, positions are grouped in sequence of significance, usually more significant towards the left.

3.1.561 Simulator. (1) A device or program used for test purposes which simulates a desired system or condition to provide proper inputs and terminations for the equipment under test. (2) A software system which predicts output results derived from a UUT functional model and user generated input stimuli.

3.1.562 Single point failure. The failure of an item which would result in failure of the system and is not compensated for by redundancy or alternative operational procedure.

3.1.563 Skew. The application of test patterns one at a time to the input contacts of a UUT in order to prevent the ATE's stimulus application method from causing race hazards to occur in the UUT during testing. Also referred to as input skew.

3.1.564 Slew or slew rate. This is the time interval required for the driver to reach the programmed voltage level. Simply defined as the slope.

3.1.565 Slewing speed. A continuous speed, usually the maximum, at which a rotating device can approach a desired location.

3.1.566 Soft failure. Failure resulting form deviations in characteristics beyond specified limits but not sufficient to cause a complete lack of function. Also referred to as a failure, soft.

3.1.567 Soft fault. (1) A fault causing a degraded performance of the UUT. (2) A condition manifested only under certain conditions of UUT operation. When those conditions change the fault disappears. Also referred to as a fault, soft.

3.1.568 Software intensive. Functions which are performed more by software than by hardware.

3.1.569 Software source documentation. Design and product specifications, source data flow charts, and descriptive data which shows how an ATE program is designed and operates its programming language, what it produces, and for what it was designed.

3.1.570 Software user documentation. Technical data instructing the operator of the test program how to load, execute and evaluate the results or products of the programs.

3.1.571 Source code. The code in which a program is prepared. Generally a high order language code (such as BASIC, ATLAS, and so forth).

3.1.572 Span. (1) The algebraic difference between the upper and lower values of a range. Notes: (A) For example: (a) Range 0 to 150, span 150: (b) Range -20 to 200, span 220: (c) Range 20 to 150, span 130: (d) Range -100 to -20, span 80. (B) The following compound terms are used with suitable modifications in the units: measured variable span, measured signal span, etc. (C) For multi-range devices, this definition applies to the particular range that device is set to measure. (2) (A) The horizontal distance between two adjacent supporting points of a conductor. (B) That part of any conductor, cable, suspension strand, or pole line between two consecutive points of support.

3.1.573 Special purpose electronic test equipment (SPETE). Electronic test equipment of a specific or peculiar nature designed to generate, modify or measure a range of electronic functions, to test a single system or equipment.

3.1.574 Special purpose test equipment (SPTE). Equipment which can only be used to test specific prime equipment.

3.1.575 Special test equipment (STE). Equipment developed for application on a specific contract for the principal purpose of providing development laboratory test capability or maintaining quality assurance of development or production end items of material. Some STE may be used for depot repair at the contractor's facility, or moved to an organic depot repair facility after completion of production.

3.1.576 Spike. An asynchronous random pulse of short duration.

3.1.577 Spike analysis. Spike analysis makes use of a mechanism in a simulator with a more accurate timing model to detect a potential spike and set the signal value to unknown or potential error for that time interval.

3.1.578 Stability. (1) An aspect of system behavior associated with systems having the general property that bounded input perturbations result in bounded output perturbations. (2) The property of retaining defined electrical characteristics for a prescribed time and environment.

3.1.579 Standard. A laboratory type device which is used to maintain continuity of value in the units of measurement by periodic comparison with higher echelon or national standards. They may be used to calibrate a standard of lesser accuracy or to calibrate test and measurement equipment directly.

3.1.580 Standard test problem. An evaluation of the performance of a system, or any part of it, conducted by setting parameters into the system; the parameters are operated on and the results obtained from system readouts.

3.1.581 Static functional test. A test in which a measurement is made of the outputs of a UUT after, and only after, these outputs have stabilized with respect to a given input stimulus. Further, the measurement and assessment is made only with respect to the specific, overall action or purpose which the UUT is intended to perform or serve.

3.1.582 Static test. A test of a non-signal property (such as direct current voltage and current), of an equipment or of any of its constituent units, performed while the equipment is energized.

3.1.583 Stimulus. Any physical or electrical input applied to a device intended to produce a measurable response.

3.1.584 Stuck fault. A failure in which the digital signal is permanently held in one of its binary states. Also referred to as a fault, stuck.

3.1.585 Subassembly. Two or more parts which form a portion of an assembly or a unit replaceable as a whole, but having a part or parts which are individually replaceable. (Examples: gun mount stand, window sash, recoil mechanism, floating piston, telephone dial, Intermediate Frequency (IF) strip, terminal board with mounted parts).

3.1.586 Supplementary data (SD). Supplementary data consists of any relevant information, text, schematics and logic diagrams necessary for analysis of the TPS and UUT in the event of a problem or anomaly during the testing process.

3.1.587 Support equipment (SE). All equipment (mobile or fixed) required to support the operation and maintenance of a material system. This includes associated multiuse end items, ground handling and maintenance equipment, tools, metrology and calibration equipment, communications resources, test equipment and automatic test equipment, with diagnostic software for both on and off equipment maintenance. It includes the acquisition of logistics support for the support and

test equipment itself. One of the principal elements of Integrated Logistic Support (ILS).

3.1.588 Support software. Software which aids in preparing, analyzing, editing, and maintaining operational or test computer programs.

3.1.589 Support system. All related facilities, equipment, material, services and personnel required for operation and maintenance of a system, so that it can be considered a self-sufficient unit in its intended operational environment.

3.1.590 Support test system. A measurement system used to assess the quality of material which consists of the following elements: (1) test equipment; (2) ancillary equipment; (3) supporting documentation; (4) physical arrangement; (5) operating environment; and (6) operating personnel.

3.1.591 Switching. The act of manually, mechanically or electrically actuating a device for opening or closing an electrical circuit.

3.1.592 Switching card. A plug-in device which provides the necessary interconnection to the UUT.

3.1.593 System integrated test (SIT). An integral capability of the mission equipment which provides an on-board, automated test capability to detect, diagnose, or isolate system failures. The fault detection/isolation (FD/I) capability is used for momentary or continuous monitoring of a system's operational health, and for observation/diagnosis as a preclude to maintenance action. System Integrated Test may be designed as an analysis tool for the overall system, integrated with several subsystems, or may be designed as an integral part of each removable component.

3.1.594 Systematic error. (1) The inherent bias (off-set) of a measurement process or (of) one of its components. (2) Error capable of identification due to its orderly character.

3.1.595 Table driven simulator. A table driven simulator operates upon the topology of the circuit, rather than compiled code. The digital circuit is stored as a set of tables indicating the fan-in list, fan-out list, value, type of gate, and so forth.

3.1.596 Tape block. A group of frames or tape lines.

3.1.597 Technical repair standard. A document which describes the UUT, tells how to test, fault-isolate, repair, and re-test the UUT.

3.1.598 Ternary simulator. A program which establishes a representation of a logic circuit or configuration based upon a computer-directed or processed simulation (or both), of the logic circuit or configuration. Node points and output pins of the simulated circuit or configuration are permitted to take on three values; logical "1", logical "0", or "X" (unknown state) in sequences and along paths in accord with program rules, in order to derive fault-detection and fault isolation information for the logic circuit or configuration represented.

3.1.599 Tertiary isolation. Isolation (usually at the depot level) at the lowest replacement level of a subunit or a component/part belonging to a subunit to return the item in question to serviceable condition. The lowest replacement level may constitute a modular assembly, printed circuit card, or a piece part.

3.1.600 Tertiary isolation level of ambiguity. The number of possible item parts (or combinations of item parts), identified by testers, test points, or manual test procedures, which must be replaced (or individually tested and then replaced) to return the item to serviceable condition. In some cases, a combination of parts (more than one part) may be required to return an item to serviceable condition. This isolation level in some instances may have to be evaluated on a qualitative basis as high, medium, or low, based on the characteristics of the item, the general test instruments required, and the effectiveness of the special instruments and testers available.

3.1.601 Test. A procedure or action taken to determine under real or simulated conditions the capabilities, limitations, characteristics, effectiveness, reliability or suitability of a material, device, system or method.

3.1.602 Test accuracy ratio (TAR). The ratio of the stimulus/measurement accuracy required to test the UUT to the accuracy of the stimulus/measurement introduced by the uncertainty of the ATE. For example, if it is required that a UUT output be accurate to 5% and the ATE/TPS accuracy in measuring the parameter is .010%, the TAR is 500.

3.1.603 Test adapter. An item providing electronic, electrical and mechanical compatibility between the UUT and the test equipment. Also referred to as a interface adapter.

3.1.604 Test analysis. The examination of the test results to determine whether the device is in a "go" or "no-go" state or to determine the reasons for or location of a malfunction.

3.1.605 Test and monitoring systems (TAMS). TAMS includes automatic testing (AT), automatic test equipment (ATE), test program sets (TPS), metrology and calibration (METCAL), diagnostics, built-in test (BIT), built-in test equipment (BITE), General Purpose Electronic Test Equipment (GPETE), Special Purpose Electronic Test Equipment (SPETE), mechanical test equipment and instrumentation, and performance monitoring hardware/software.

3.1.606 Test bench. Equipment specifically designed to provide a suitable work surface for testing a unit in a particular test setup under controlled conditions.

3.1.607 Test chamber. An enclosure which is specifically designed to provide connectors, adapters, and stimulus for performing a test under a controlled environment.

3.1.608 Test comprehension. The ability of a test program to detect faults, expressed as percentage of total faults.

3.1.609 Test coverage. Ratio of defects actually capable of diagnosis by the tester to total defects in the fault spectrum.

3.1.610 Test diagram. An interconnecting diagram of the ATE and UUT interface, depicting the hookup and active signal lines required for enacting a test or group of tests.

3.1.611 Test effectiveness. Measures which include consideration of hardware design, BIT design, test equipment design, and TPS design. Test effectiveness measures include, but are not limited to, fault coverage, fault isolation, fault detection time, fault isolation time, and false alarm rate.

3.1.612 Test equipment. Electric, electronic, mechanical, hydraulic, or pneumatic equipment (either automatic, manual, or any combination thereof) which is required to perform the monitoring, fault detection, and fault isolation functions.

3.1.613 Test fixture. An item providing electronic, electrical, pneumatic, etc. and mechanical compatibility between the UUT and the test equipment.

3.1.614 Test generation. The process of generating tests or test stimuli.

3.1.615 Test language. A language specifically designed to express one or more aspects of automatic testing.

3.1.616 Test logic. The logical, systematic examination of circuits and their diagrams to identify and analyze the probability and consequence of potential malfunctions for determining related maintenance or maintainability design requirements.

3.1.617 Test, measurement and diagnostic equipment (TMDE). Any system or device used to evaluate the operational condition of an end item or subsystem thereof, or to identify and/or isolate any actual or potential malfunction. TMDE includes diagnostic and prognostic equipment, semiautomatic and automatic test equipment (with issued software), and calibration test or measurement equipment.

3.1.618 Test pattern. (1) The pattern of logic states to be applied to the inputs of a digital UUT by a digital tester (usually automatic). (2) A stimulus design to exercise the UUT transfer function.

3.1.619 Test point. An electrical contact designed into a circuit specifically for the measurement of internal signals so as to increase the testability of the circuit.

3.1.620 Test point selector. A device capable of selecting test points on a UUT in accordance with instructions from the test program.

3.1.621 Test procedure. A document that describes step by step the operations required to test a specific item. A test procedure can be UUT-oriented or test equipment-oriented.

3.1.622 Test program (TP). The TP contains the coded sequence which, when executed by the ATE, will provide ATE a set of instructions sufficient to automatically ascertain the operational condition of a UUT and detect and isolate faults within the UUT.

3.1.623 Test program instruction (TPI). The TPI provides information needed for testing (e.g., hook-up, probe point locations or other programmed operator intervention) which cannot be conveniently provided by the ATE under control of the TP. Appropriate contents are largely dependent on the ATE being used.

3.1.624 Test program integration. The initial mating of an ATE, a TPS and a UUT to assure functional performance (debug).

3.1.625 Test program set (TPS). A TPS consists of those items necessary to test a Unit Under Test (UUT) on an ATE. This includes the electrical, mechanical, instructional and logical decision elements. The individual elements of the TPS are TP, ID and TPSD.

3.1.626 Test program set document (TPSD). A TPSD consists of the printed information, not provided by the ATE, which is necessary to determine the operational condition and perform fault detection and fault diagnostics of a UUT on an ATE. The individual elements of the TPSD shall be the TPI and Supplementary Data (SD). TPSD data is required for support at the Intermediate Level of maintenance.

3.1.627 Test program set integration. TPS integration is that phase in the development of a TPS by which the developer interfaces the TPS elements with the UUT and ATE for the purpose of debugging the TPS. This integration is accomplished prior to TPS validation.

3.1.628 Test program set validation and verification. TPS validation is that process in the development of the TPS by which the correctness of the program is eval-uated by running it on the ATE together with the UUT and its appropriate ID. The process includes the identification of the run-time errors, procedure errors and other errors, or omissions inhibiting test performance. The process is accomplished by actual fault insertion on the UUT. The process is performed in accordance with approved quality assurance criteria. Verification by the cognizant activity constitutes a First Article acceptance of all elements of a TPS in accordance with MIL-STD-2077 and the work authorization document.

3.1.629 Test programming procedures. Documents which explain in detail the composition of test programs including definitions and logic used to compose the program. These procedures also provide instructions to implement changes in the program.

3.1.630 Test provisions. The capability included in the design for conveniently evaluating the performance of (and locating the faulty item in) a system, subsystem, set, group, unit, assembly, or subassembly.

3.1.631 Test requirement specification. A specification developed to establish contractual requirements for test documentation, TPSs, and test verification and validation.

3.1.644 Testability. A design characteristic which allows status (operable, inoperable, or degraded) of an item to be determined and the isolation of faults within the item to be performed in a timely manner.

3.1.645 Testability measurement. A measurement of the ease and adequacy of testing derived as a result of demonstration or field operation.

3.1.646 Testability prediction. A prediction of the ease and adequacy of testing developed through use of models or schematics (or both). The prediction is based on parameters such as fault detection, fault isolation, and MTTR.

3.1.647 Threshold sensitivity. The smallest quantity that can be detected by an electronic item (such as a radio receiver, a measuring instrument, or an automatic control system).

3.1.648 TMDE register. A listing of TMDE technical descriptions of items for use in determining which proposed or fielded TMDE can be applied to fulfill the TMDE requirements of equipment programs, thus insuring maximum use of in-service assets and elimination of duplicate development or procurement of similar items of TMDE for different system applications.

3.1.649 Tolerance. The total permissible deviation of a measurement from a designated value.

3.1.650 Topologically independent faults. Two faults are said to topologically independent if the set of signal lines in the circuit which can be affected by the value of the signal line where one fault is located does not intersect that of the other. That is, these faults can not affect any common portion of the circuit. Topologically independent faults can therefore be simulated simultaneously to speed up processing.

3.1.651 TPS validation. The testing of a UUT using the TPS developed for the UUT in order to validate that the TPS meets its design.

3.1.652 TPS verification. The testing of a UUT using the TPS developed for the UUT in order to verify that the TPS meets its requirements.

3.1.653 Traceability. The ability to relate individual measurement results to national standards or nationally accepted measurement systems through an unbroken chain of comparisons.

3.1.654 Traceability life. Historic testing documentation through the life of a unit.

3.1.655 Transducer. (1) A device that is actuated by power from one system and supplies power in any other form to a second system. (2) A device by means of which energy can flow from one or more transmission systems or media to one or more other transmission systems or media. Note: The energy transmitted by these systems or media may be of any form (for example, it may be electric, mechanical, or acoustical), and it may be of the same form or different forms in the various input and output systems or media. (3) A device to receive energy from one system and supply energy, of either the same or of a different kind, to another system, in

3.1.632 Test requirements analysis. The examination of test requirements to determine adequacy, range of test stimuli, measurements, method of test (such as manual or automated), and type of test equipment.

3.1.633 Test requirements document. A specification document which contains the required performance characteristics and interfacing requirements for a unit under test (UUT) and specifies the tests, conditions, values (and associated tolerances) of the stimuli and associated responses needed to: (a) indicate a properly operating UUT; (b) detect and indicate all faults and out of tolerance conditions; (c) adjust and align the UUT (when applicable); and (d) isolate each fault or out of tolerance condition to the assembly indenture level and degree of ambiguity necessary to effect repair or adjustment of the UUT consistent with the established maintenance concept. (Note that unambiguous fault isolation is usually desired but is not always economically justifiable.)

3.1.634 Test sequence. The order in which tests or test patterns are run.

3.1.635 Test sequence number. Identification of a position in a test sequence.

3.1.636 Test software. An aggregate of the test programs peculiar to an ATE or TMDE designed to accomplish the test function of a UUT automatically.

3.1.637 Test specification. A document which specifies the required performance characteristics, interface requirements, tests, test conditions and values (and associated tolerances) of the stimuli and associated responses needed to test a UUT for a particular test objective (for example, production acceptance, etc.).

3.1.638 Test spectrum. A range of test stimuli and measurements based on analysis or prime equipment test requirements.

3.1.639 Test stand. An equipment specifically designed to provide suitable mountings, connections, and controls for testing electrical, mechanical, or hydraulic equipment as an entire system.

3.1.640 Test strategy. The arrangement of specific tester types to achieve optimum throughput and diagnostic capability at the least possible cost given the fault spectrum process yield, production rate and product mix for a particular production environment.

3.1.641 Test support software. Computer programs used to prepare, analyze, and maintain test software.

3.1.642 Test validation. A process in the production of a test program by which the correctness of the program is assured by running it on the ATE together with the UUT.

3.1.643 Test verification. The Government performance of a test in accordance with a test procedure to demonstrate that the test set-up (and the test procedure) covers the test requirements of the UUT.

such a manner that the desired characteristics of the energy input appear at the output. (4) A device which under the influence of a change in energy level of one form or in one system, produces a specified change in energy level of another form or in another system.

3.1.656 Transient failure. A temporary failure induced by a momentary or temporary external factor such as input power fluctuation, excessive ambient temperature excursion, electromagnetic interference, or by factors internal to a system. Also referred to as a failure, transient.

3.1.657 Trunk. A single circuit between two points, both of which are switching centers and individual distribution points.

3.1.658 Turn-on BIT. A specific type of initiated BIT which is exercised each time power is applied to the unit or system. Also referred to as BIT turn-on.

3.1.659 Uncertainty. The estimated amount by which the observed or calculated value of a quantity may depart from the true value. Note: The uncertainty is often expressed as the average deviation, the probable error, or the standard deviation.

3.1.660 Undershoot. The amount by which a pulse amplitude exceeds (negatively) some set reference value after it has changed its state. Also, considered a distortion which occurs after a major pulse transition.

3.1.661 Unit delay simulation. A digital logic simulation technique which assumes that the propagation delay time for all primitives is the same.

3.1.662 Unit under test (UUT). A UUT is any system, set, subsystem, assembly or subassembly undergoing testing.

3.1.663 Unknown state. Most memory elements used in sequential circuits are bistable devices. When the power is turned on, they can assume either one of the two stable states. Because they are normally designed to have a symmetrical configuration, the initial states become unpredictable and are called unknown states. Unknown states can also be the result of critical races or oscillations.

3.1.664 Utility software. Computer programs used for directory manipulation, memory management, disc I/O, test I/O, error message output, interrupt routines, and miscellaneous I/O.

3.1.665 Validation. That process in the production of a test program by which the correctness of the program is verified by running it on the automatic test equipment together with the Unit Under Test. The process includes the identification of run-time errors, procedure errors, and other non-compiler errors, not covered by pure software methods.

3.1.666 Variable delay simulation. A digital logic simulation technique which allows the user to fix the propagation delay time for each usage of a primitive element.

3.1.667 Verification. The procedure for verifying that the deliverable item meets its contractual requirements.

3.1.668 Vertical standardization. The use of the same test procedure (or TPS) and associated test set-up (or ATE) at several support levels.

3.1.669 Vertical test compatibility. The condition which exists when test results are usable and consistent across different levels of maintenance. To achieve vertical test compatibility, controlled (tested) parameters of the UUT must be consistent and the parameter tolerance hierarchy must be consistent across the maintenance levels. Failure to achieve vertical test compatibility results in RTOKs.

3.1.670 Wait. A programmed instruction which causes an automatic test system to remain in a given state for a predetermined period.

3.1.671 Waveform digitizer. A measurement instrument which contains sampling analog to digital converters, memory storage and internal processing capability. Digitized data can also be transferred to a computer for further processing.

3.1.672 Weapon replaceable assembly (WRA). A generic term which includes replaceable packages of a system installed in the weapon system with the exception of cables, mounting provisions, and fuse boxes or circuit breakers.

3.1.673 Wire data list. Tabular listing indicating point-to-point wire runs and connections of an interface adapter, UUT or other device.

3.1.674 Wrap-around test. Self-test of an ATE system or test instrument accomplished by connecting the system's outputs to its inputs, usually through a self-test adaptor or built-in switching network.

3.1.675 Zero delay simulation. A digital logic simulation technique which assumes that all circuit devices have no propagation delay.

3.1.676 Z-state or high impedance state. A logic level that a node is set at when all outputs connected to that node are deactivated or turned off.

3.2 Acronyms used in this standard. The acronyms in this Military Standard are defined as follows:

a. ABIT - Automatic Built-In-Test
b. ACE - Automatic Check-out Equipment
c. AME - Automatic Monitoring Equipment
d. AT - Automatic Testing
e. ATE - Automatic Test Equipment
f. ATG - Automatic Test Generator
g. ATLAS - Abbreviated Test Language for All Systems
h. ATPG - Automatic Test Program Generator
i. BIT - Built-In-Test
j. BITE - Built-In-Test Equipment
k. BNF - Backus-Naur Form

l. C/ATLAS - Common Abbreviated Test Language for All Systems
m. CAD - Computer Aided Design
n. CAGE - Commercial and Government Entity
o. CND - Cannot Duplicate
p. CPI - Calibration Procedure Instruction
q. CTP - Calibration Test Program
r. CTPS - Calibration Test Program Set
s. EAROM - Electronically Alterable Read Only Memory
t. EPROM - Erasable Programmable Read Only Memory
u. ESD - Engineering Support Data
v. FD/I - Fault Detection/Isolation
w. FIR - Functional Item Replacement
x. FMEA - Failure Modes and Effects Analysis
y. FMECA - Failure Modes and Effects and Criticality Analysis
z. GPETE - General Purpose Electronic Test Equipment
aa. GPIB - General Purpose Interface Bus
ab. IBIT - Initiated BIT
ac. ID - Interface Device
ad. ID - Integrated Diagnostics
ae. IF - Intermediate Frequency
af. ILS- Integrated Logistic Support
ag. I/O - Input/Output
ah. LRU - Line Replaceable Unit
ai. LRU - Lowest Replaceable Unit
aj. METCAL - Metrology and Calibration
ak. MTBF - Mean Time Between Failures
al. MTPSI - Master Test Program Set Index
am. MTTR - Mean Time To Repair
an. NAVDEP - Naval Aviation Depot
ao. OTP - Operational Test Program
ap. OTPH - Operational Test Program Hardware
aq. OTPI - Operational Test Program Instruction
ar. OTPM - Operational Test Program Medium
as. OTPS - Operational Test Program Set
at. PBIT - Power-on BIT
au. PME - Precision Measurement Equipment
av. R&M - Reliability and Maintainability
aw. RAM - Random Access Memory
ax. ROM - Read Only Memory
ay. RTOK - Re-Test OK
az. SD - Supplementary Data
ba. SE - Support Equipment
bb. SIT - System Integrated Test
bc. SPETE - Special Purpose Electronic Test Equipment
bd. SPTE - Special Purpose Test Equipment
be. SRA - Shop Replaceable Assembly
bf. SRU - Shop Replaceable Unit
bg. STE - Special Test Equipment
bh. TAMS - Test and Monitoring Systems
bi. TAR - Test Accuracy Ratio
bj. TMDE - Test, Measurement and Diagnostic Equipment
bk. TP - Test Program

bl. TPI - Test Program Instruction
bm. TPS - Test Program Set
bn. TPSD - Test Program Set Document
bo. TRD - Test Requirements Document
bp. TSR - Test Strategy Report
bq. UUT - Unit Under Test
br. WRA - Weapon Replaceable Assembly

4. GENERAL REQUIREMENTS

4.1 Purpose of TMDE definitions. It is intended that TMDE definitions be up-to-date as used by military and industry experts in each respective field or area. Their primary purpose is to provide users with a standard definition essential to the development of various written documents for the military. At the same time, they are intended to identify and limit the terms used in the TMDE community to those definitions designated and preferred or standard in order to constrain the proliferation of definitions.

5. DETAILED REQUIREMENTS

5.1 This section is not applicable to this standard.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. This standard contains definitions of key words and terms used in testing, measurement, and diagnostics.

6.2 Acquisition requirements. Acquisition documents must specify the following:

(a) Title, number, and date of this standard.
(b) Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1.1).

6.3 Subject term (key word) listing.

Acronyms
Coordinated terms
Standardization
Test machinery
Troubleshooting

6.4 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - SH
Air Force - 99

Review Activities:
Army - MI
Navy - AS, MC
Air Force - 11, 17

User Activities:
Army - ME
Navy - CG, OS, YD

Preparing Activity:
Navy - SH
(Project ATTS-8903)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-STD-1309D	2. DOCUMENT DATE (YYMMDD) 12 FEBRUARY 1992

3. DOCUMENT TITLE
DEFINITIONS OF TERMS FOR TESTING, MEASUREMENT AND DIAGNOSTICS

4. NATURE OF CHANGE *(Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)*

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle Initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) (1) Commercial (2) AUTOVON (If applicable)	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME Technical Point of Contact (TPOC): Ms. M. Dymond (SEA 04DS4) PLEASE ADDRESS ALL CORRESPONDENCE AS FOLLOWS:	b. TELEPHONE (Include Area Code) (1) Commercial: TPOC: 703-602-2224 (2) AUTOVON: 8-332-2224
c. ADDRESS (Include Zip Code) Commander, Naval Sea Systems Command Department of the Navy (SEA 55Z3) Washington, DC 20362-5101	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340